EN 202 Electronics

Welcome

My Introduction

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Your Introduction

- Name
- Place
- Background of electronics and electrical
- What you expect from this course

Objective of course

To give you a basic background of electronics engineering, which is required for

- Troubleshooting, understanding and making of electrical/electronics circuits/instruments
- Understanding of basic terminology of electronics
- For laboratory experiments
- Minimum electronics knowledge which help in understanding system in which electronics is one of the component

Digital Electronics

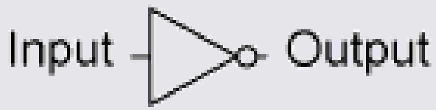
References

- A.P. Malvino and D.P. Leach, Digital Principles and Applications, Tata McGraw Hill Edition
- W.H. Gothmann, Digital Electronics – An Introduction to Theory and Pratice, Prentice Hall of India Private Limited.
- A. P. Malvino, J. A. Brown, Electronics : An Introduction to Microcomputers, Tata Mcgraw Hill.

Logic Gates

NOT Gate OR Inverter

NOT gate truth table

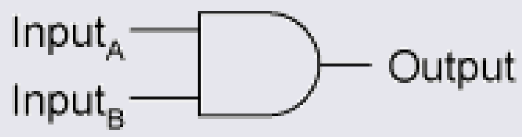


Input	Output
0	1
1	0

Logic - Opposite of input

AND Gate

AND gate

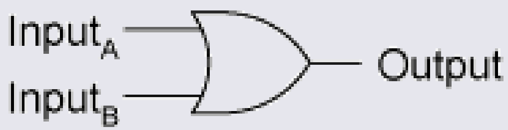


A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Logic – output is 0 if there is any input 0

OR Gate

OR gate

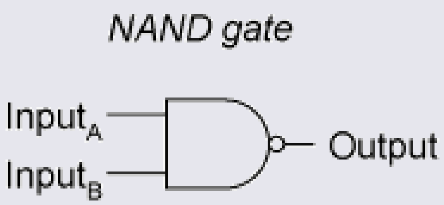


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Logic – output is 1 if there is any input 1

NAND Gate

Universal Gate

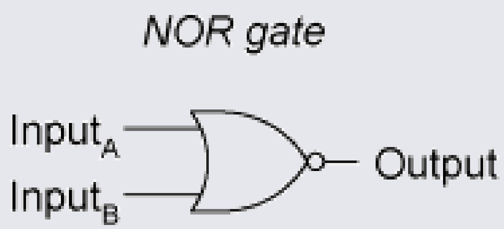


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Logic – output is 1 if there is any input 0

NOR Gate

Universal Gate

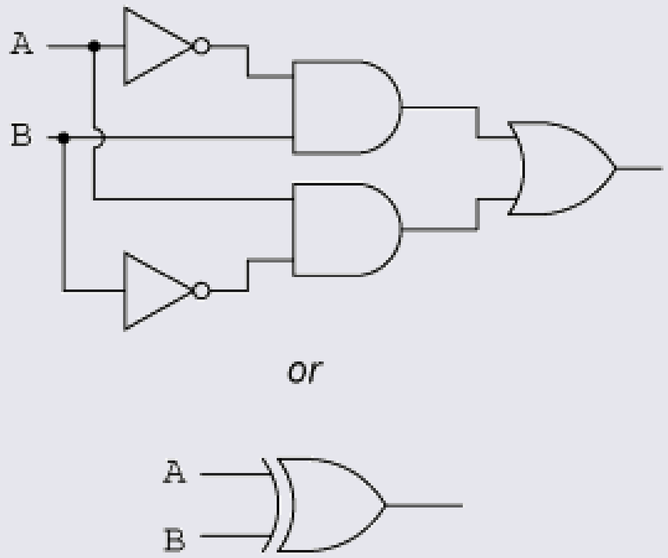


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Logic – output is 0 if there is any input 1

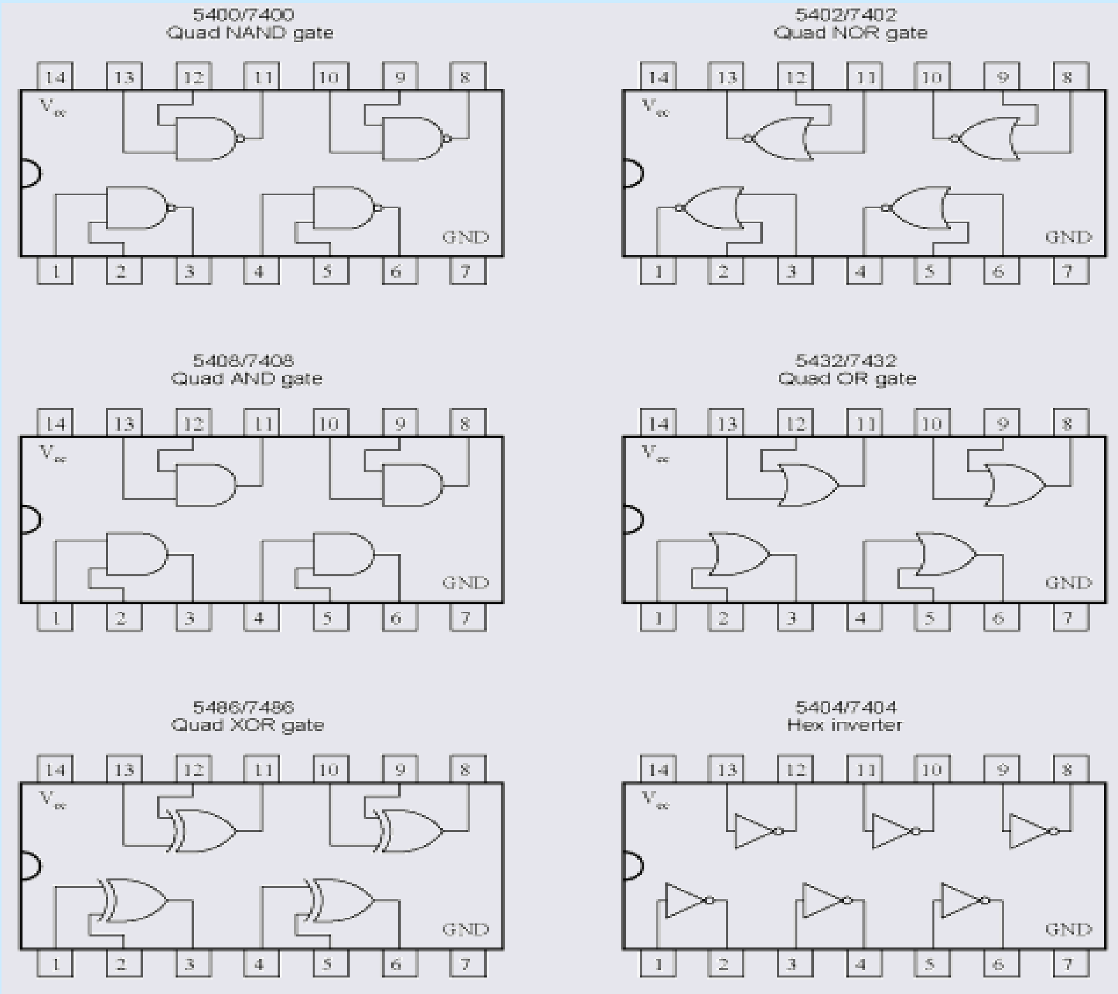
XOR Gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



Logic – output is 1 if there are odd number of 1’s in input

IC’s of logic gates



Problem

- Construct NOT, OR and AND function by NAND Gate

Problem

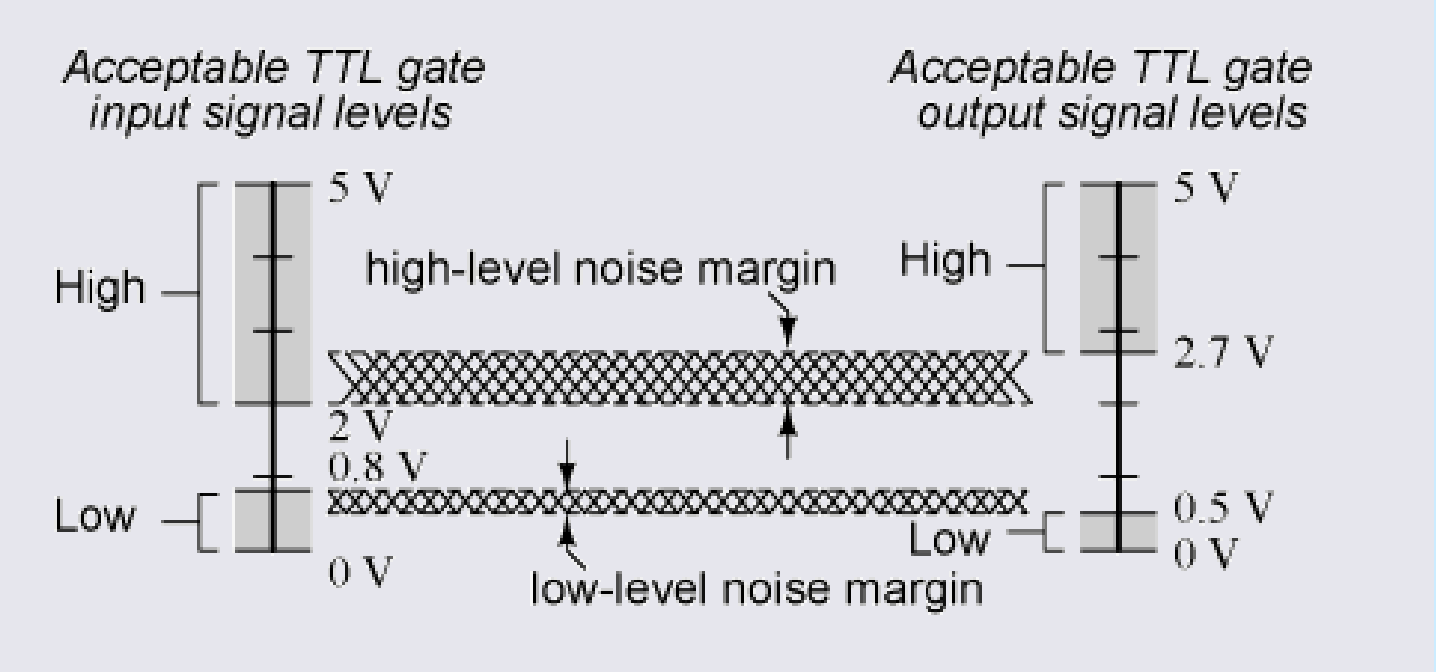
- Construct NOT, OR and AND function by NOR Gate

Problem

Propose an application based on digital circuit

Acceptable input & output voltage

TTL – Transistor-Transistor Logic



Binary number system

- Why binary number system is required in digital electronics ?
  - Only two states are possible
- Decimal Odometer
  - 000, 001, 002, 003...009, 010, 011..099, 100, 101
- Binary Odometer
  - 000, 001, 010, 011, 100, 101, 110, 111
- Bit = X
- Nibble= XXXX
- Byte = XXXX XXXX

MSB LSB

Weight of digits

Decimal	Binary
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111
16	10000
17	10001
18	10010
19	10011
20	10100

- Weigh of digit in decimal system

```
1206 = 1000 + 200 + 6
1206  =  (1 x 1000) + (2 x 100) + (0 x 10) + (6 x 1)
```

- Weight of digit in binary

Convert 11001101_2 to decimal form:

```
bits =          1  1  0  0  1  1  0  1
.               -  -  -  -  -  -  -  -
weight =        1  6  3  1  8  4  2  1
(in decimal     2  4  2  6
notation)       8
```

Problems

- A number 7 is required to electrically transmit from one town to another town. What are possible ways ?
- Convert 10101 to decimal
- Convert 55 to binary
  - Successive division

Binary addition

```
0 + 0 = 0
1 + 0 = 1
0 + 1 = 1
1 + 1 = 10
1 + 1 + 1 = 11
```

Examples

```
                           11  1 <--- Carry bits ----->  11
  1001101                 1001001                        1000111
+ 0010010               + 0011001                      + 0010110
---------               ---------                      ---------
  1011111                 1100010                        1011101
```

Binary subtraction

0-0=0

1-0=1

1-1=0

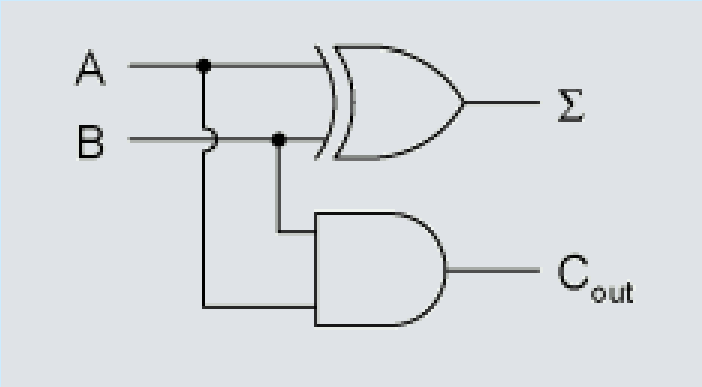
10-1=1

Examples

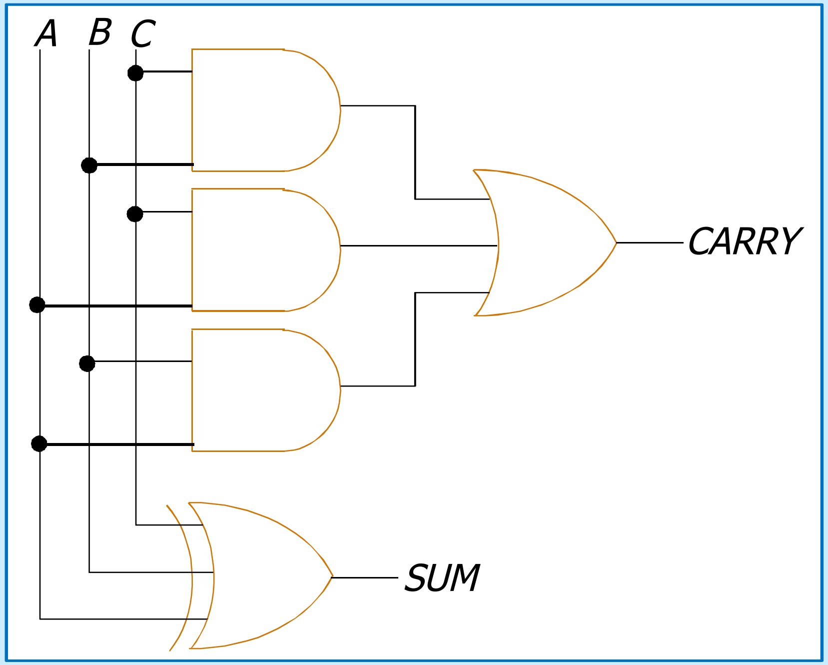
407	100 (4)	1101 (13)	11001000
-328	-001 (1)	-1010 (10)	-01001011
------	---------	--------------	--------------
079	011 (3)	0011 (3)	01111101

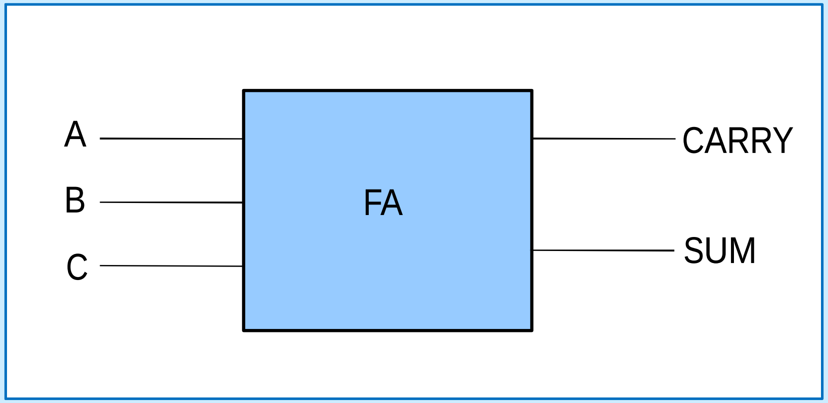
Binary Adder

Half Adder



Full Adder

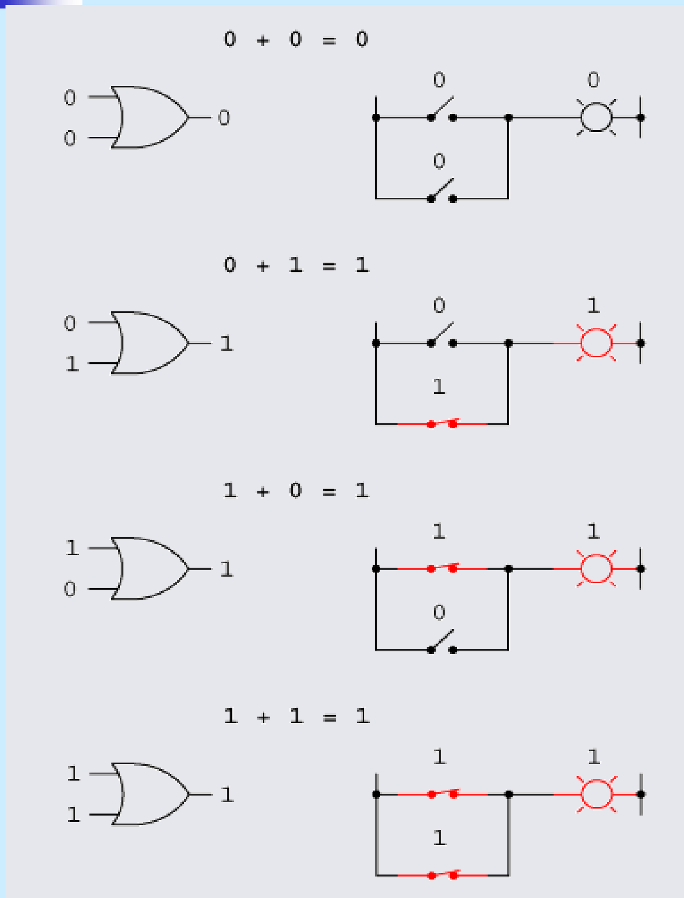




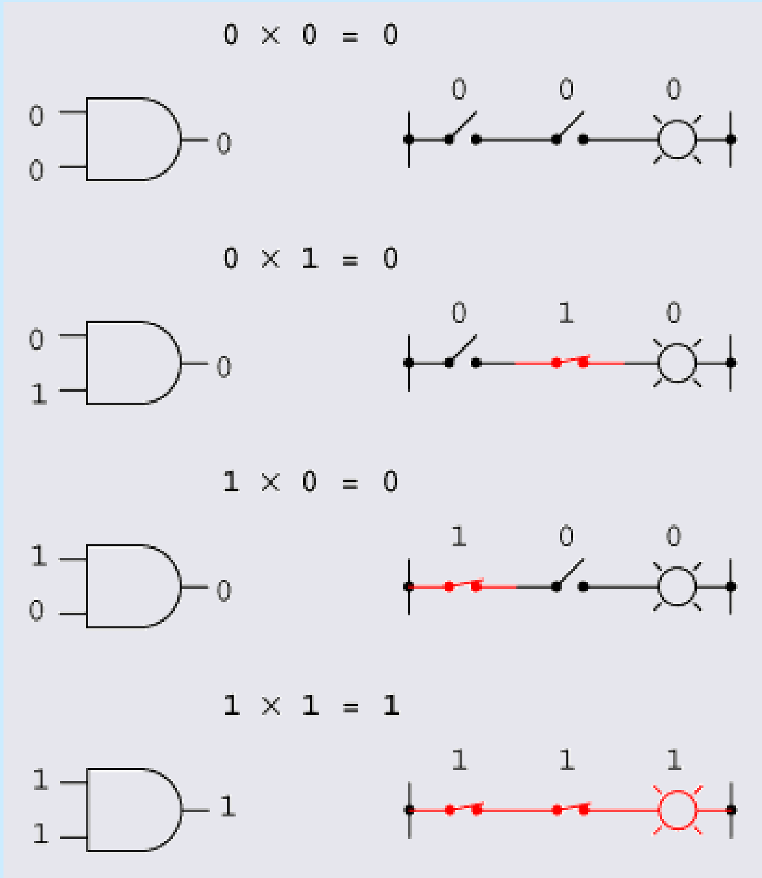
Boolean Arithmetic

- Based on logic gate

OR and AND operation



Y= A+B



Y= A.B

NOT, NAND and NOR

- NOT
  - $Y = \overline{A}$
- NAND
  - $Y = \overline{AB}$
- NOR
  - $Y = \overline{A + B}$
- XOR
  - Y = ??

Basics of boolean algebra

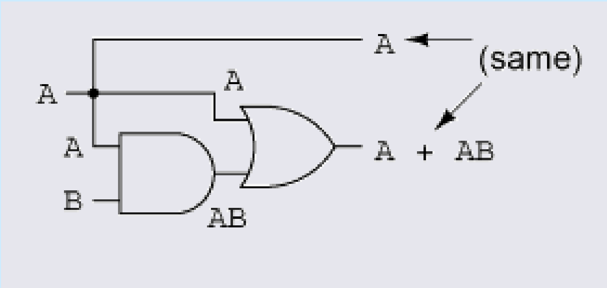
Additive	Multiplicative
$A + 0 = A$	$0A = 0$
$A + 1 = 1$	$1A = A$
$A + A = A$	$AA = A$
$A + \overline{A} = 1$	$A\overline{A} = 0$

Additive	Multiplicative
$A + B = B + A$	$AB = BA$
$A + (B + C) = (A + B) + C$	$A(BC) = (AB)C$

$$A(B + C) = AB + AC$$

Boolean rules for simplification

- $A + AB = A$



$A + AB$

Factoring A out of both terms

$A(1 + B)$

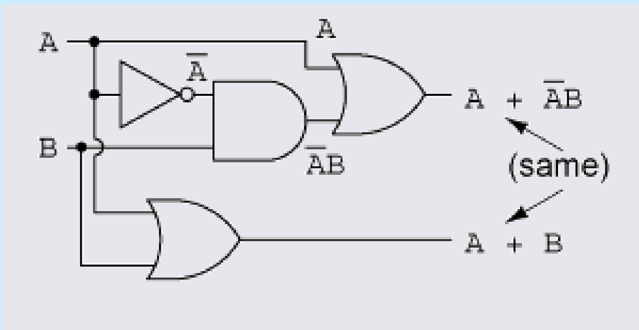
Applying identity $A + 1 = 1$

$A(1)$

Applying identity $1A = A$

A

- $A + \overline{A}B = A + B$



$A + \overline{A}B$

Applying the previous rule to expand A term

$A + AB = A$

$A + AB + \overline{A}B$

Factoring B out of 2nd and 3rd terms

$A + B(A + \overline{A})$

Applying identity $A + \overline{A} = 1$

$A + B(1)$

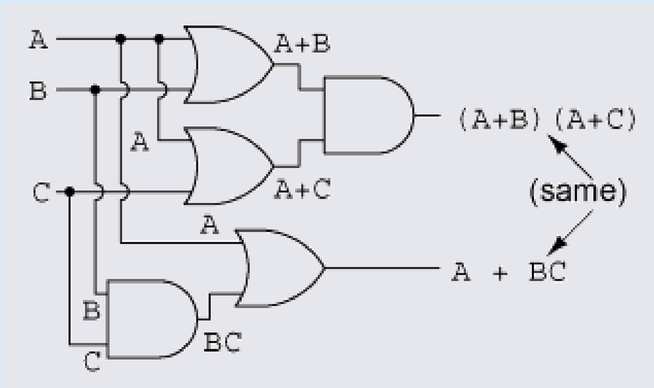
Applying identity $1A = A$

$A + B$

Truth table's should match

Contd.

- $A+BC=(A+B)\,(A+C)$



$(A + B)(A + C)$

↓ Distributing terms

$AA + AC + AB + BC$

↓ Applying identity $\mathbf{AA} = \mathbf{A}$

$A + AC + AB + BC$

↓ Applying rule $\mathbf{A} + \mathbf{AB} = \mathbf{A}$ to the $A + AC$ term

$A + AB + BC$

↓ Applying rule $\mathbf{A} + \mathbf{AB} = \mathbf{A}$ to the $A + AB$ term

$A + BC$

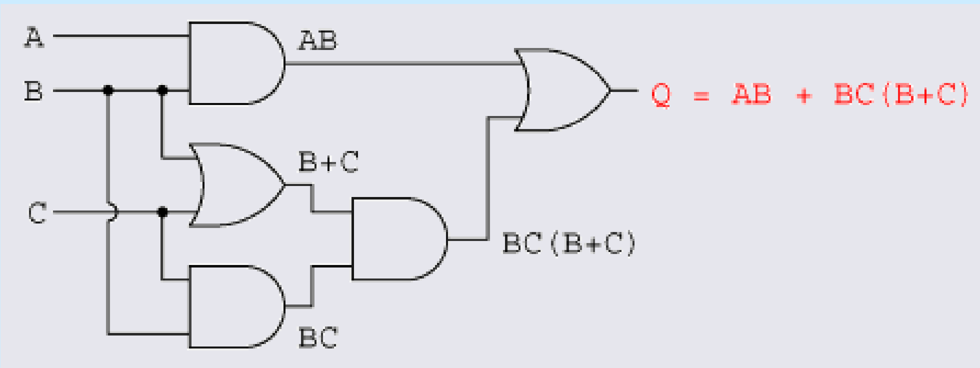
Useful Boolean rules for simplification

$A + AB = A$

$A + \overline{A}B = A + B$

$(A + B)(A + C) = A + BC$

Circuit simplification example



$AB + BC(B + C)$

↓ Distributing terms

$AB + BBC + BCC$

↓ Applying identity $AA = A$ to 2nd and 3rd terms

$AB + BC + BC$

↓ Applying identity $A + A = A$ to 2nd and 3rd terms

$AB + BC$

↓ Factoring B out of terms

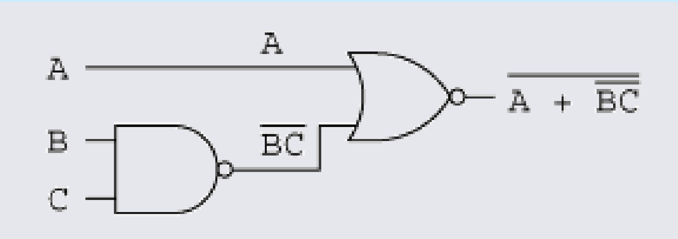
$B(A + C)$

Realize with less number of gates

DeMorgan's Theorems

DeMorgan's Theorems

break!	*break!*
$\overline{AB}$	$\overline{A + B}$
$\downarrow$	$\downarrow$
$\overline{A} + \overline{B}$	$\overline{A}\,\overline{B}$
NAND to Negative-OR	*NOR to Negative-AND*



$$\overline{A + \overline{BC}}$$

$\downarrow$ Breaking longest bar (addition changes to multiplication)

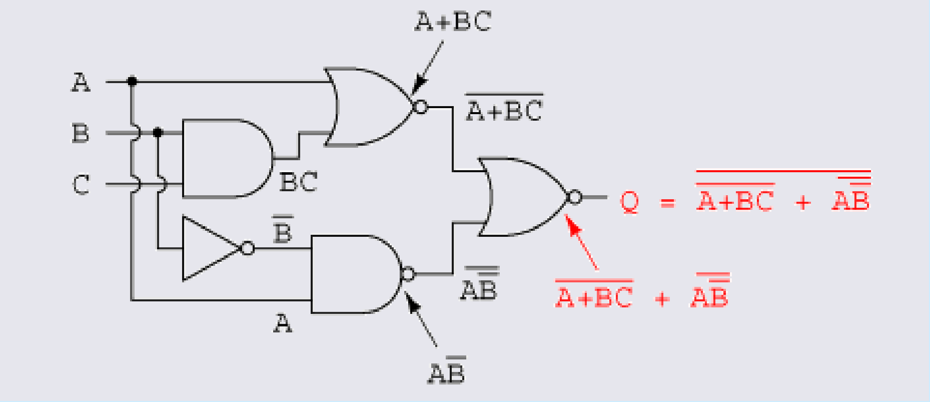
$$\overline{A}\;\overline{\overline{BC}}$$

$\downarrow$ Applying identity $\overline{\overline{A}} = A$ to $\overline{\overline{BC}}$

$$\overline{A}BC$$

Problem

- Solve



- Ans $A\overline{B}$

Problems

$$\overline{\overline{AB} + \overline{A} + AB +} = 0$$

$$AB + \overline{AC} + A\overline{B}C(AB + C) = 1$$

Converting truth tables into Boolean expressions

Sum of product approach

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

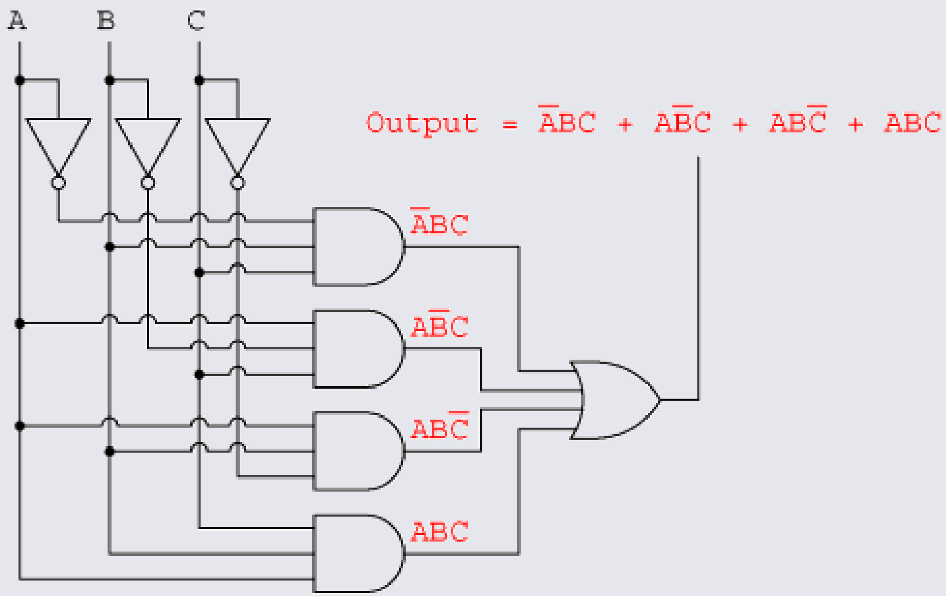
$\overline{A}BC = 1$

$A\overline{B}C = 1$

$AB\overline{C} = 1$

$ABC = 1$

$\text{Output} = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

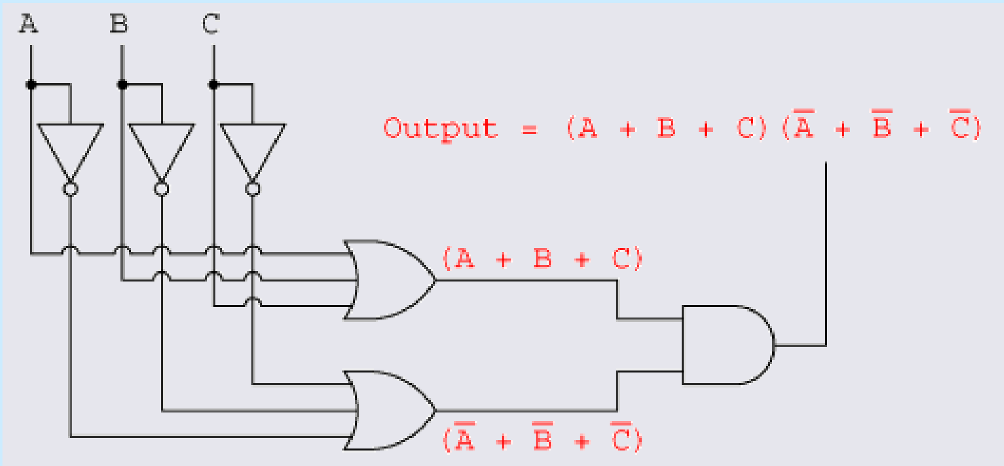


Ans AB+BC+CA

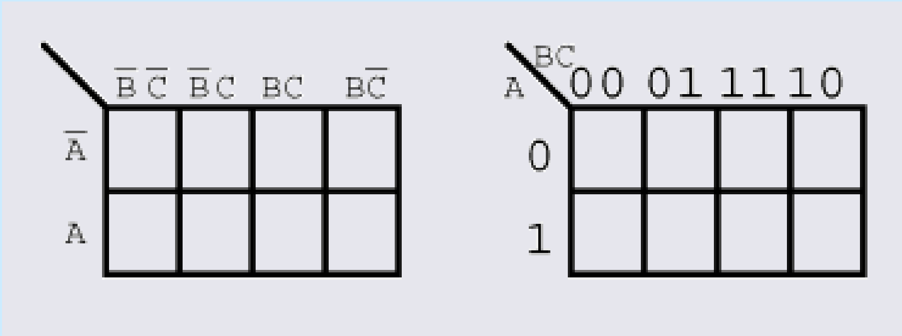
Contd.

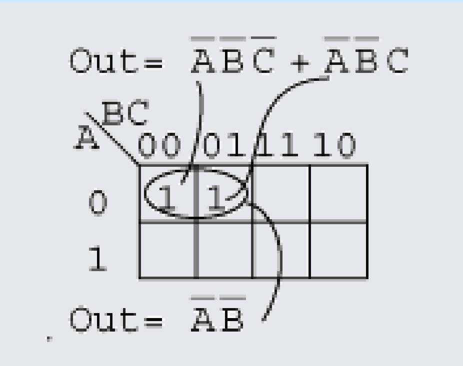
Product-Of-Sums approach

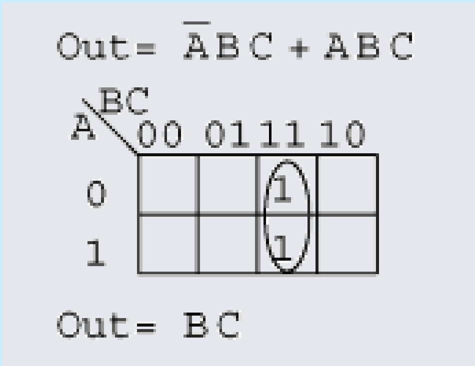
A	B	C	Output	
0	0	0	0	$(A + B + C)$
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	1	
1	0	1	1	
1	1	0	1	
1	1	1	0	$(\overline{A} + \overline{B} + \overline{C})$

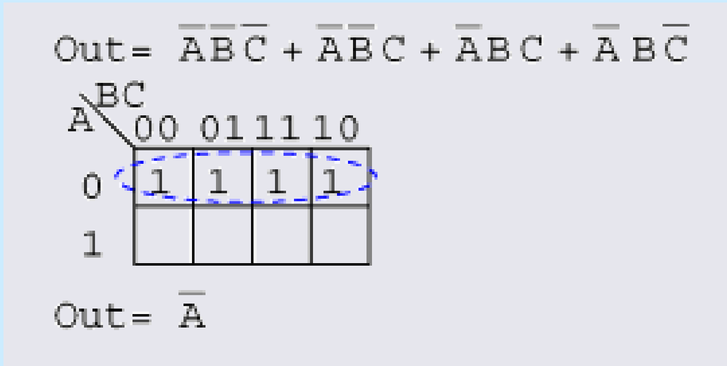


Logic simplification with Karnaugh maps



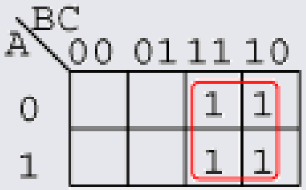






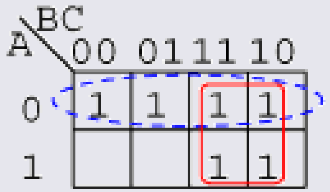
Contd.

Out = $\bar{A}BC + \bar{A}B\bar{C} + ABC + AB\bar{C}$



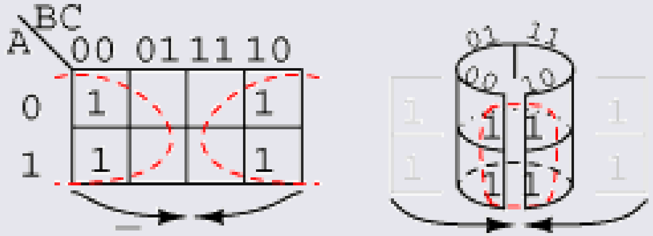
Out = B

Out = $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + ABC + AB\bar{C}$



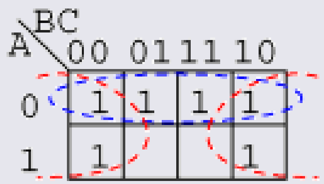
Out = $\bar{A} + B$

Out = $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C}$



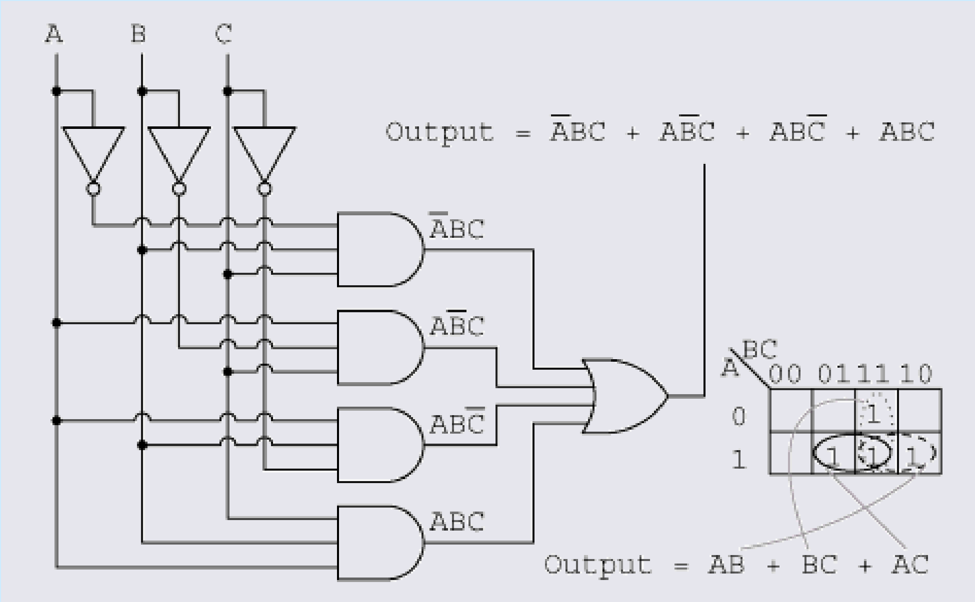
Out = $\bar{C}$

Out = $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$

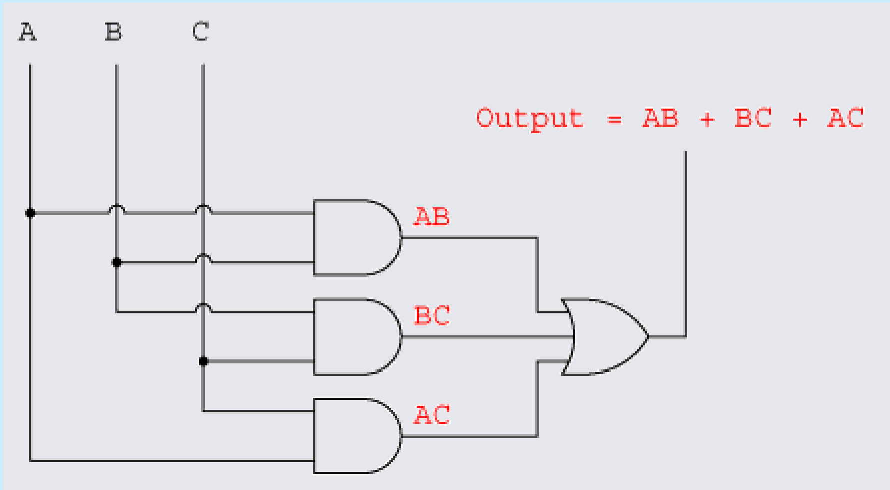


Out = $\bar{A} + \bar{C}$

Contd.

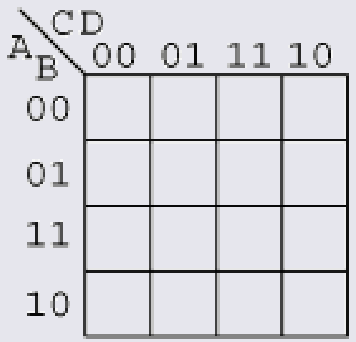


A
B
C
Output = $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$
$\bar{A}BC$
$A\bar{B}C$
$AB\bar{C}$
ABC
BC
A
00 01 11 10
0
1
1
1 1 1
Output = AB + BC + AC

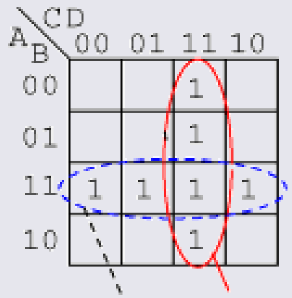


A
B
C
Output = AB + BC + AC
AB
BC
AC

Larger 4-variable Karnaugh maps

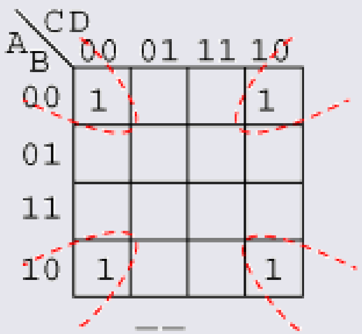


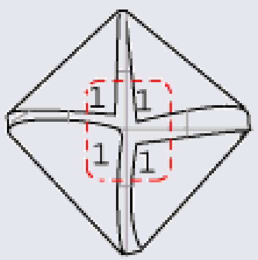
Out= $\overline{A}\,\overline{B}CD + \overline{A}BCD + ABCD + A\overline{B}CD + AB\overline{C}\,\overline{D} + AB\overline{C}D + ABC\overline{D}$



Out= AB + CD

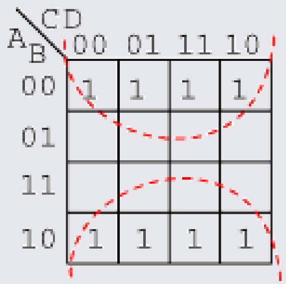
Out= $\overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}C\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C\overline{D}$





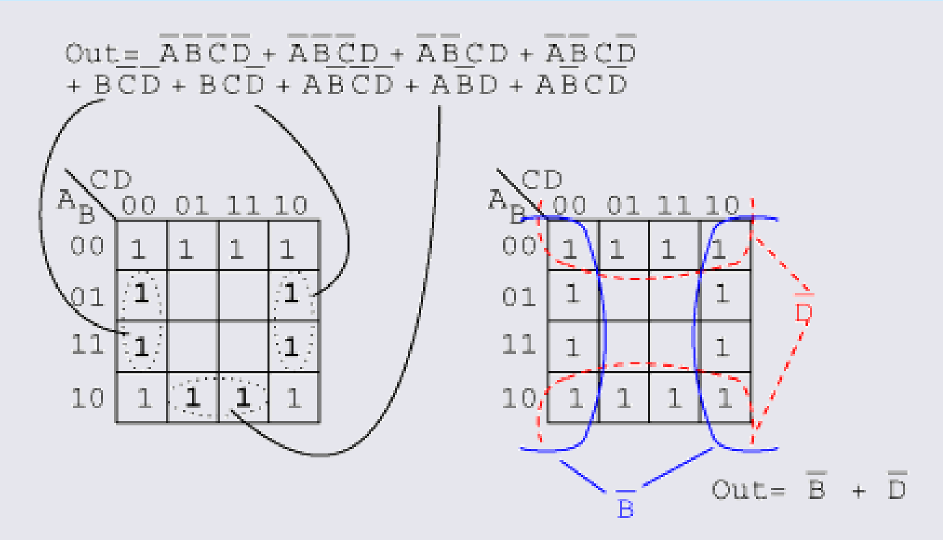
Out= $\overline{B}\,\overline{D}$

Out= $\overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D}$
$+ A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}D + A\overline{B}CD + A\overline{B}C\overline{D}$

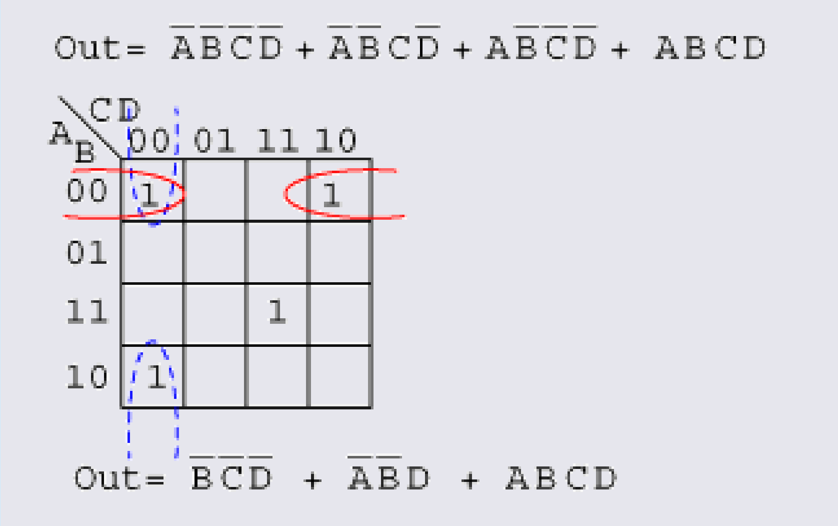


Out= $\overline{B}$

Contd.



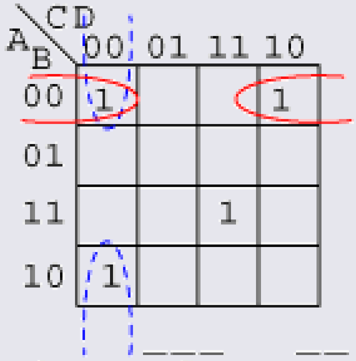
$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D}$
$+ B\overline{C}\,\overline{D} + BC\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}D + A\overline{B}C\overline{D}$
CD
AB
00 01 11 10
00 1 1 1 1
01 1 1
11 1 1
10 1 1 1 1
$\overline{D}$
$\overline{B}$
$Out = \overline{B} + \overline{D}$



$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}C\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + ABCD$
CD
AB
00 01 11 10
00 1 1
01
11 1
10 1
$Out = \overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{D} + ABCD$

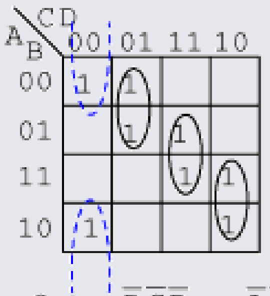
Contd.

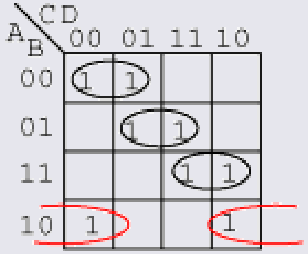
$Out = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + ABCD$



$Out = \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + ABCD$

$Out = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + \bar{A}BCD$
$+ ABCD + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D}$



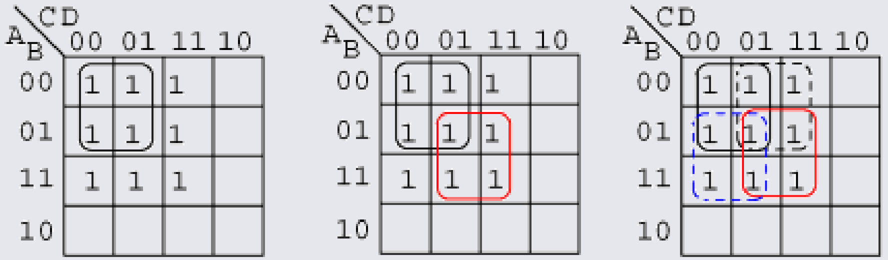


$Out = \bar{B}\bar{C}\bar{D} + \bar{A}\bar{C}D + BCD + AC\bar{D}$

$Out = \bar{A}\bar{B}\bar{C} + \bar{A}BD + ABC + A\bar{B}\bar{D}$

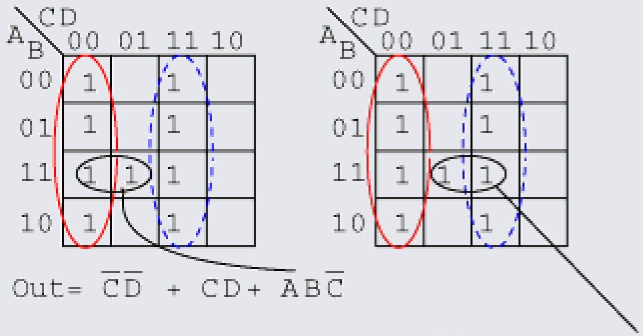
Contd.

$Out = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
$+ \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BCD$
$+ AB\bar{C}\bar{D} + AB\bar{C}D + ABCD$



$Out = \bar{A}\bar{C} + \bar{A}D + B\bar{C} + BD$

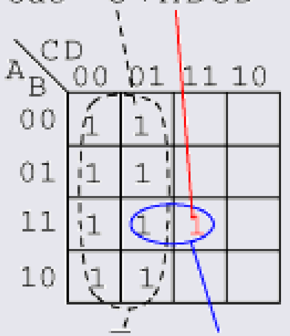
$Out = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D}$
$+ AB\bar{C}D + ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD$



$Out = \bar{C}\bar{D} + CD + AB\bar{C}$

$Out = \bar{C}\bar{D} + CD + ABD$

$Out = \bar{C} + ABCD$



$Out = \bar{C} + ABD$

Simplification by Boolean Algebra

$Out = \bar{C} + ABCD$

Applying rule $A + \bar{A}B = A + B$ to the $\bar{C} + ABCD$ term

$Out = \bar{C} + ABD$

Sigma Notation

$$\begin{aligned}Out = \;&\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD\\ &+ \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BCD\\ &+ AB\bar{C}\bar{D} + AB\bar{C}D + ABCD\end{aligned}$$

$$f(A,B,C,D) = \sum m(0,1,3,4,5,7,12,13,15)$$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	0	0	0

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	0	0	0

$$f(A,B,C,D) = \bar{A}\bar{C} + \bar{A}D + B\bar{C} + BD$$

Pi-Notation

$f(A,B,C,D) = \prod M(2,6,8,9,10,11,14)$

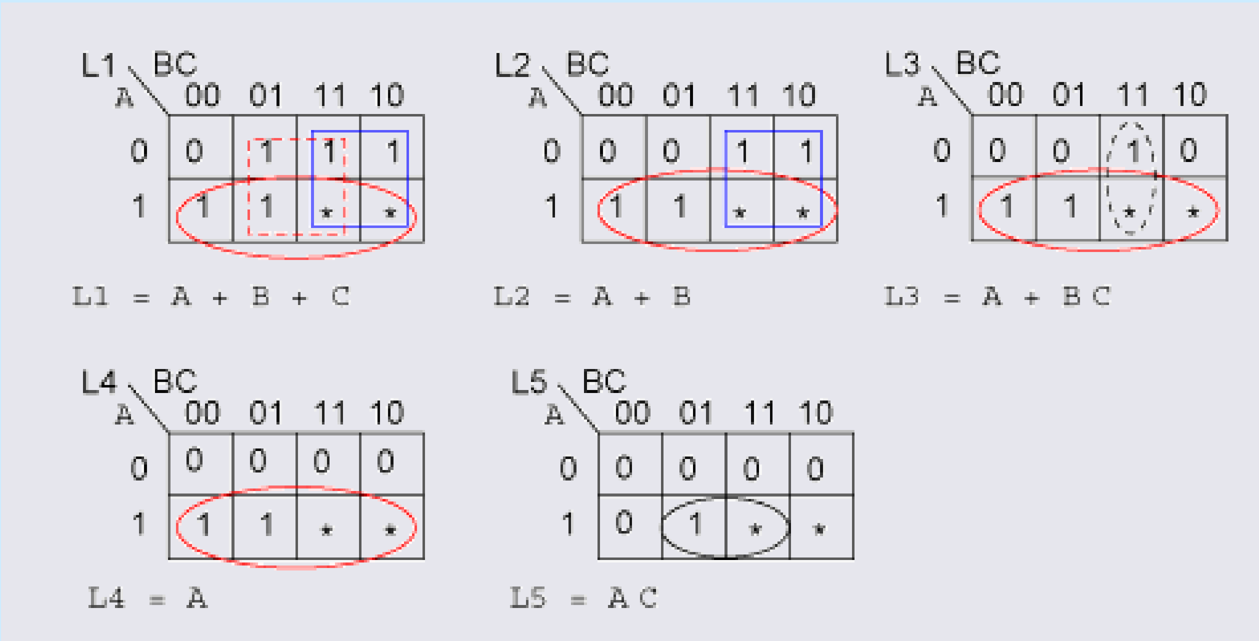
AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	0	0	0

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	0	0	0

$f(A,B,C,D) = (\overline{A}+B)(\overline{C}+D)$

Don't Care cells in the Karnaugh map



Problem

$f = \Sigma\, m\ (0,1,3,4,5,7,10,13)$

$f = \Sigma\, m\ (1,2,3,5,6,7,8,12,13)$

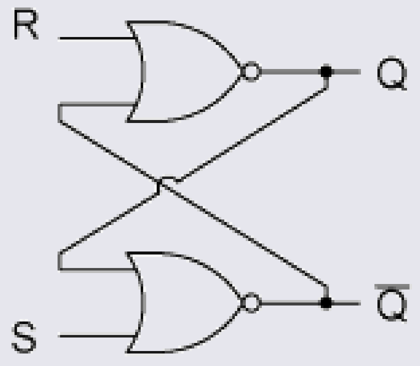
$f = \Sigma\, m\ (0,2,6,10,11,12,13) + d(3,4,5,14,15)$

FLIP-FLOP

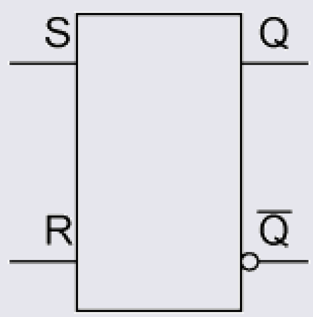
Sequential logic

Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history

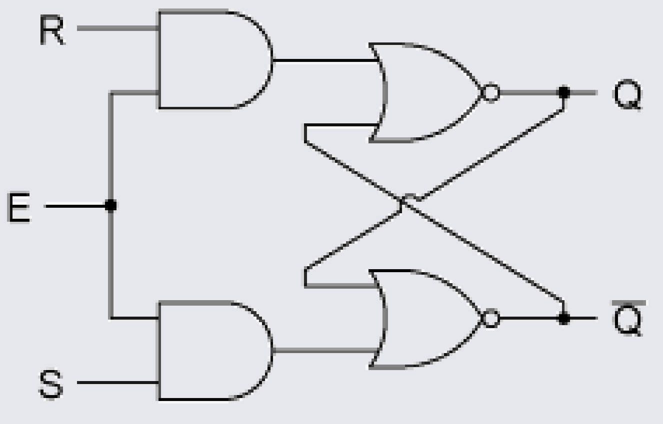
R-S Flip-flop or R-S latch



S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

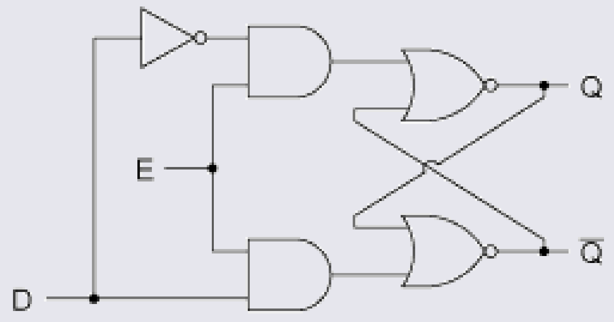


Gated S-R latch

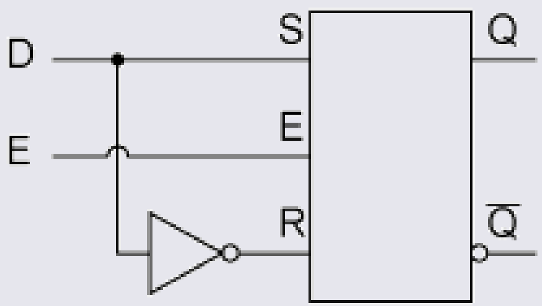


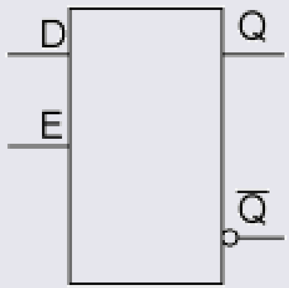
E	S	R	Q	$\overline{Q}$
0	0	0	latch	latch
0	0	1	latch	latch
0	1	0	latch	latch
0	1	1	latch	latch
1	0	0	latch	latch
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

D Flip-flop OR D latch

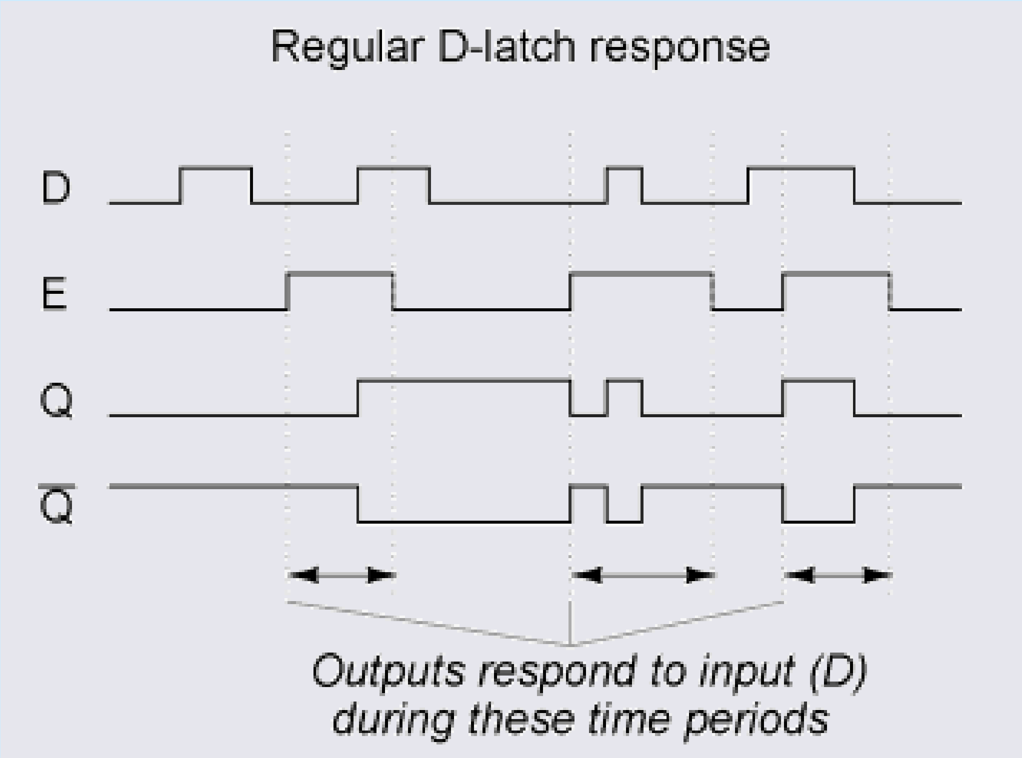


E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

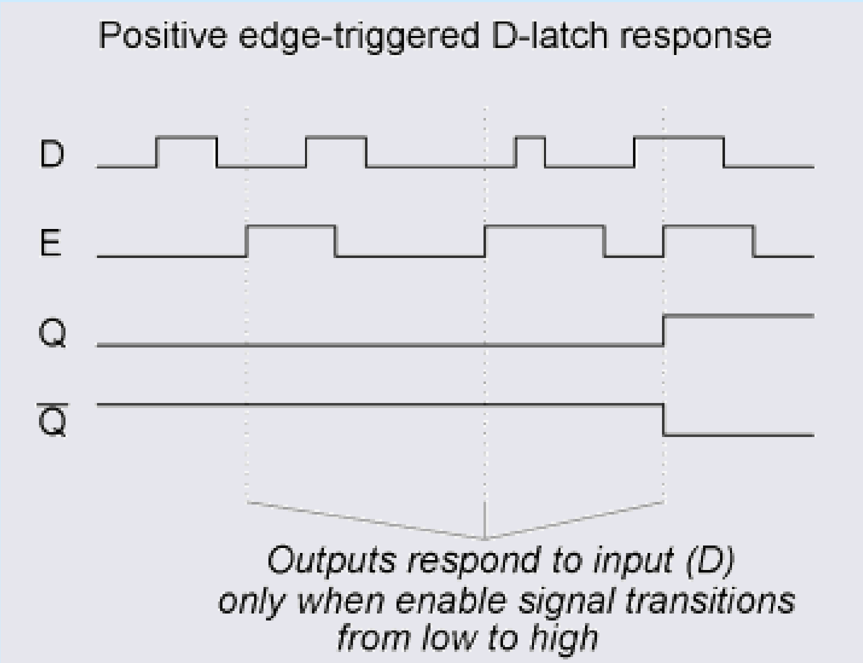


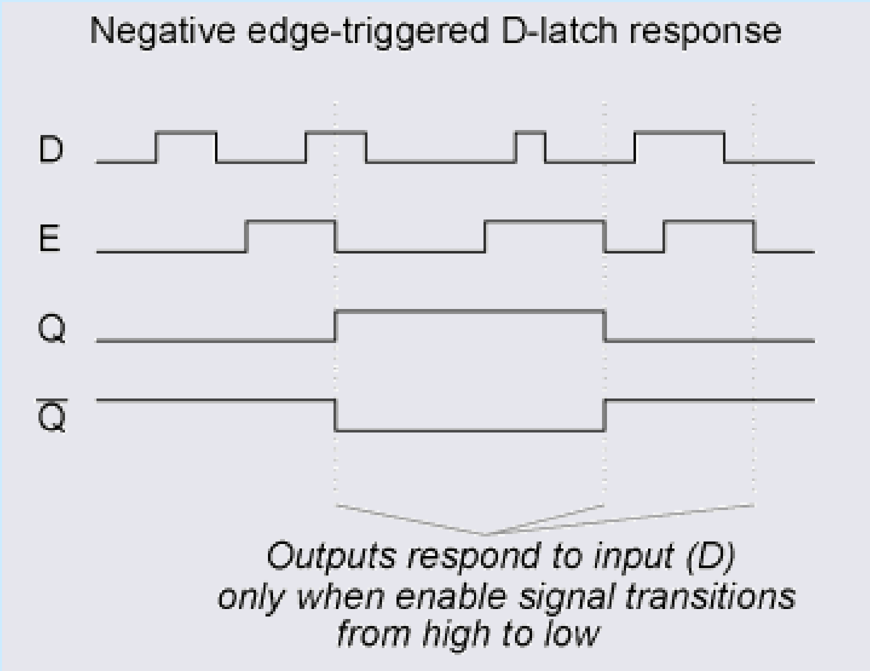


D Flip-Flop Response

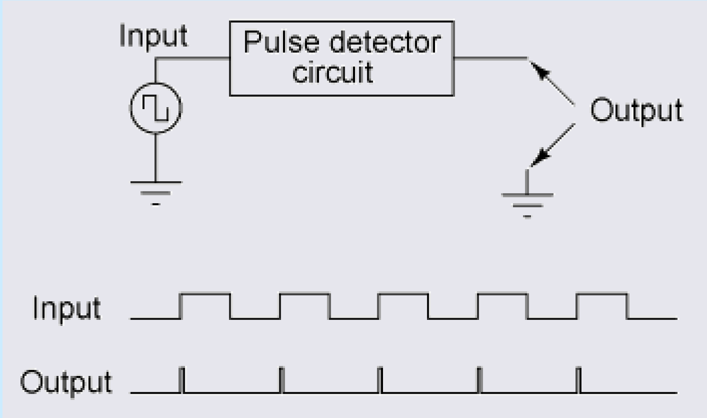


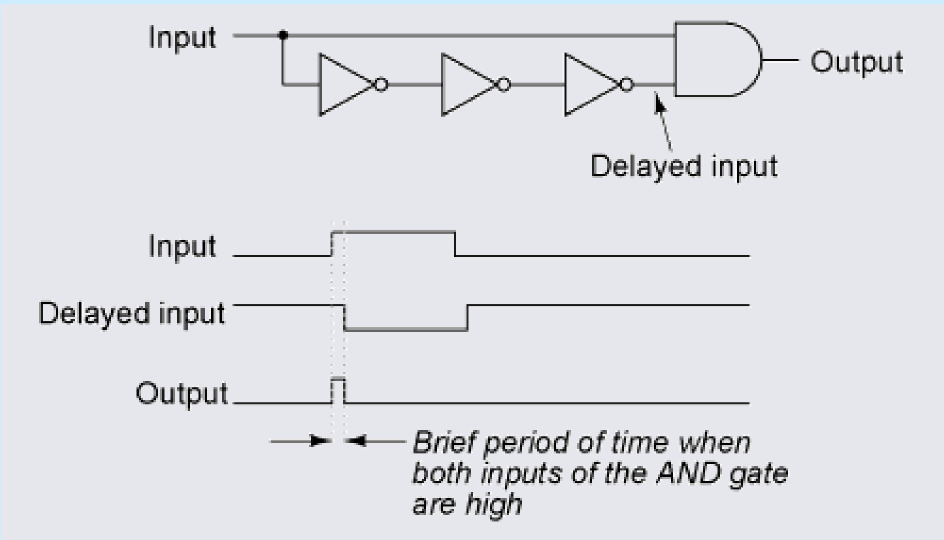
Edge-triggered Response

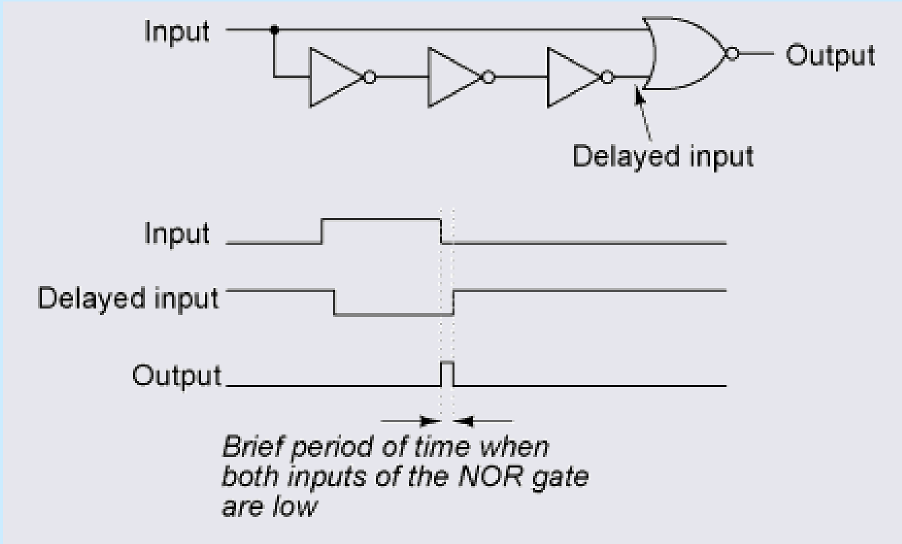




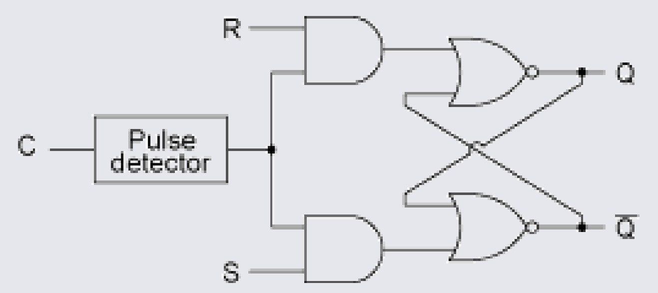
Edge trigger realization



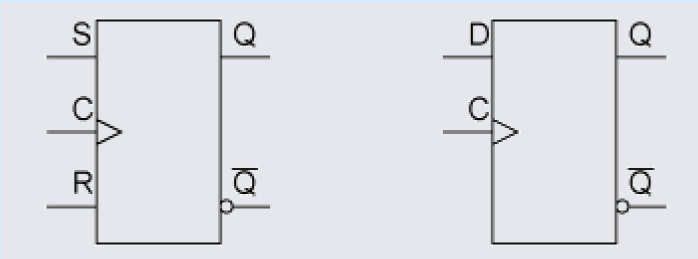


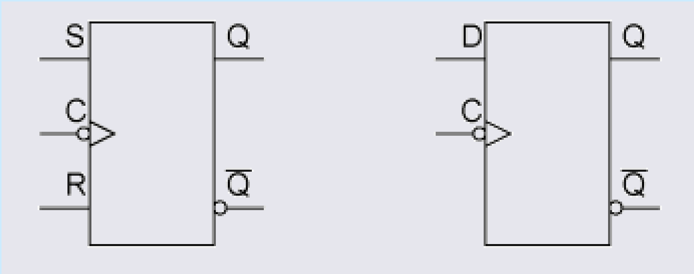


Edge triggered RS flip-flop

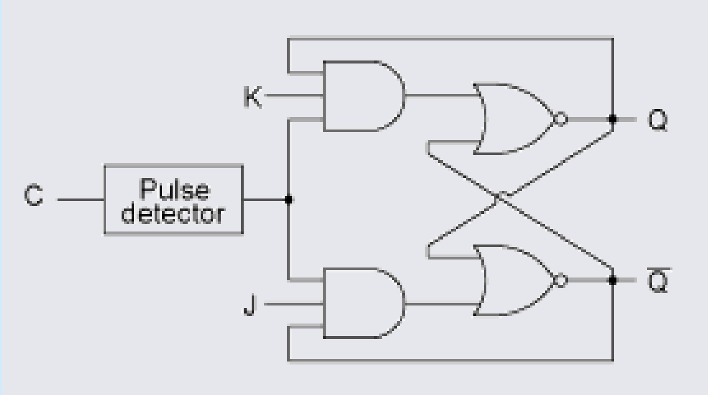


C	S	R	Q	$\overline{Q}$
↑	0	0	latch	latch
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	0	0
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

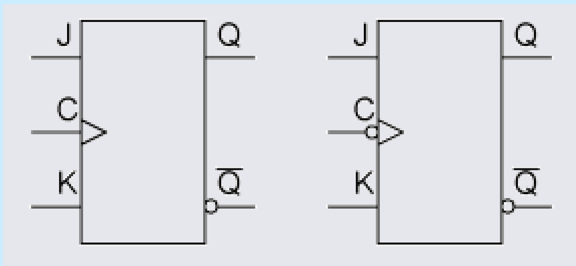




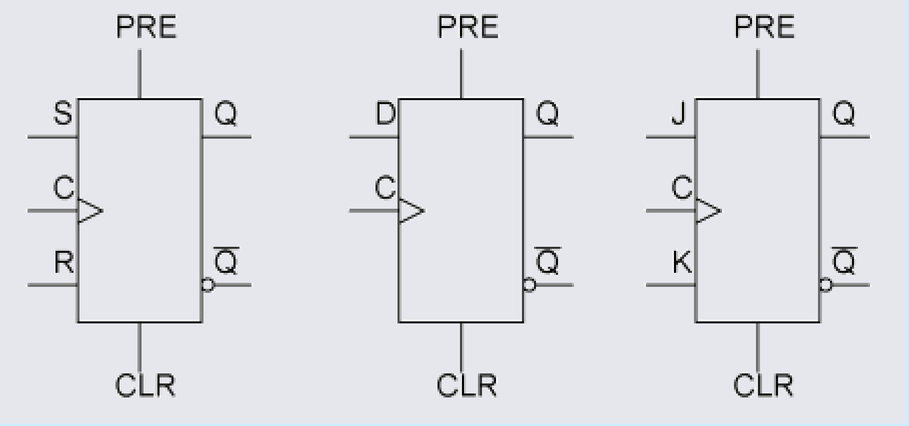
J-K flip-flop

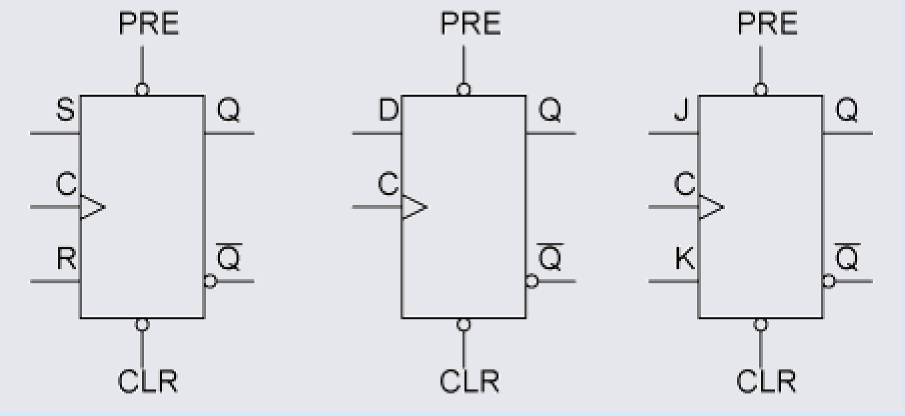


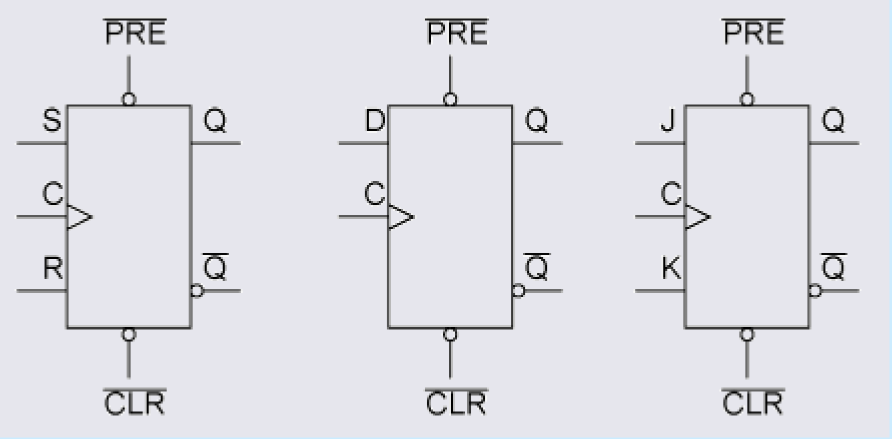
C	J	K	Q	$\overline{Q}$
↑	0	0	latch	latch
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch



Preset and Clear in flip-flop

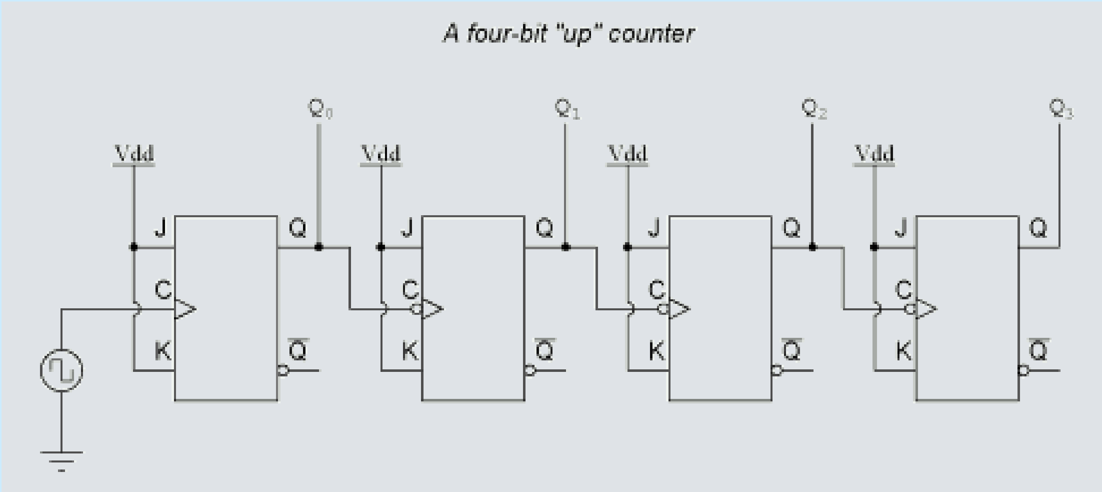


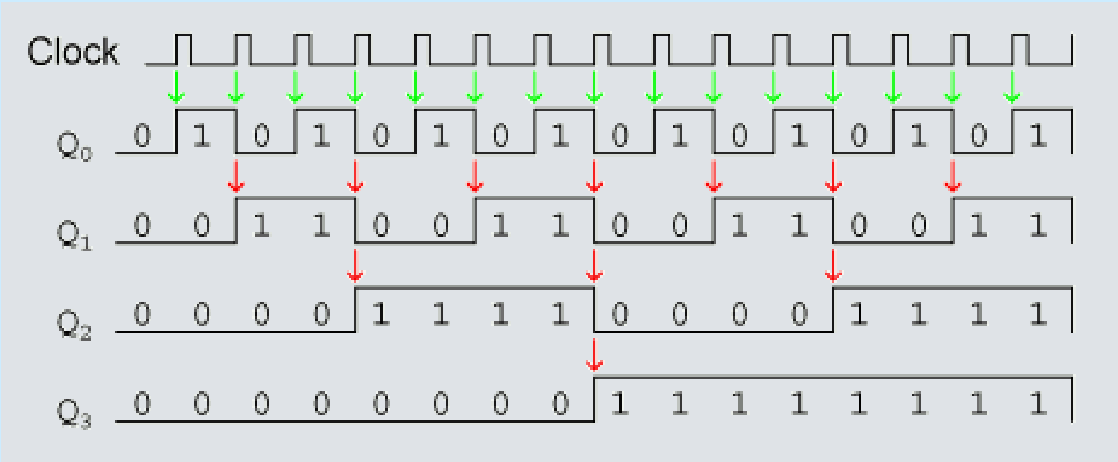




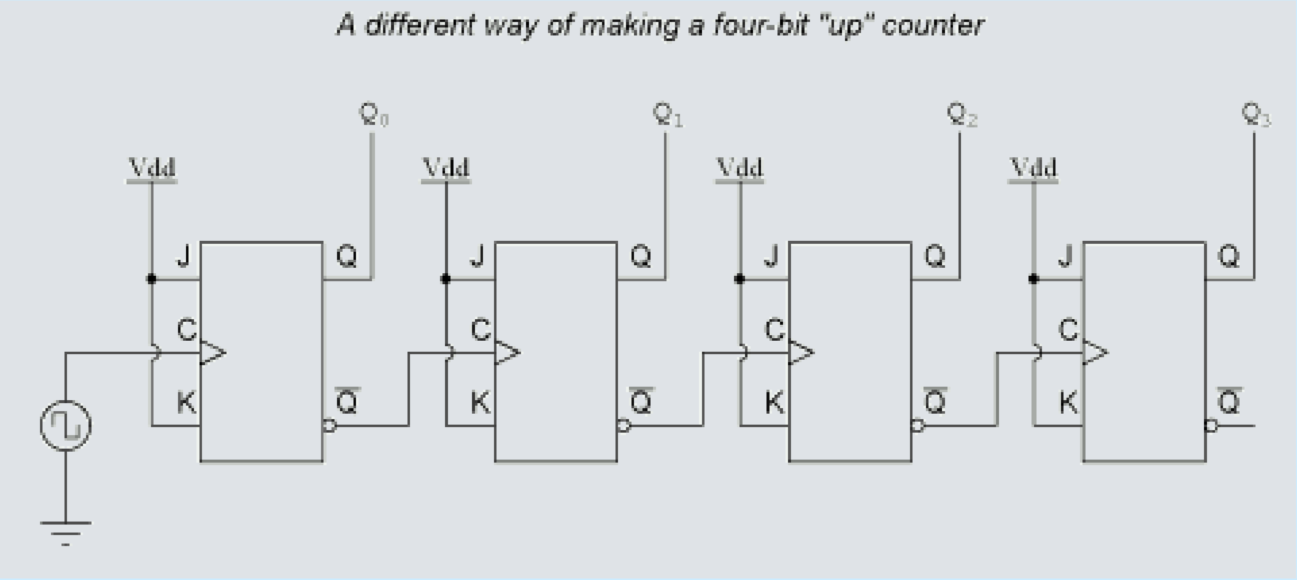
Counters

Asynchronous counters





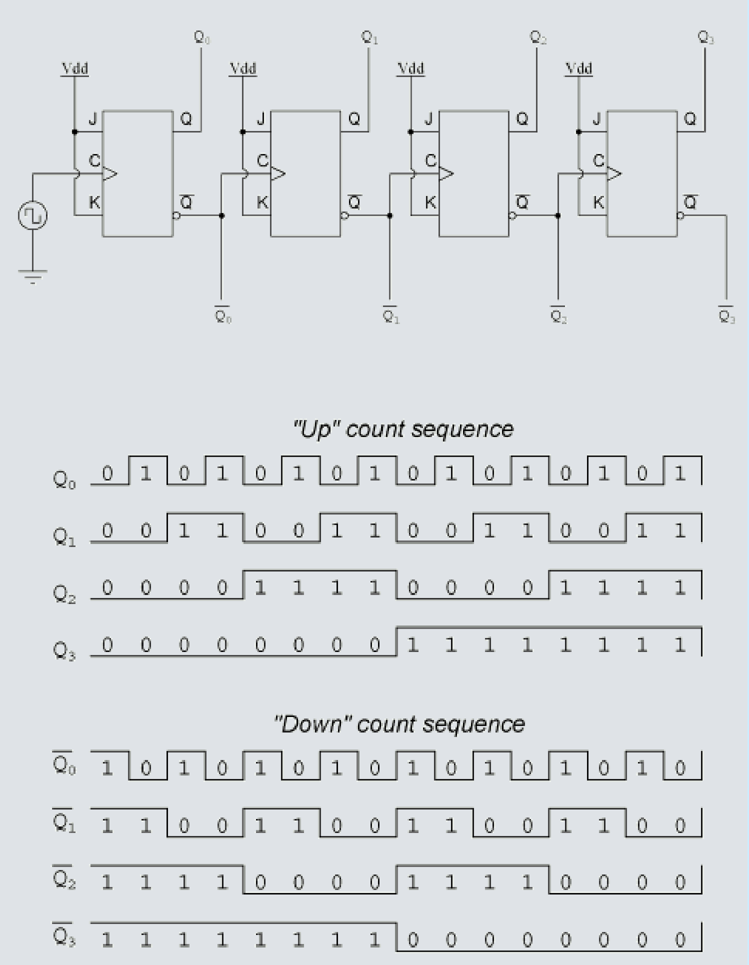
Contd.



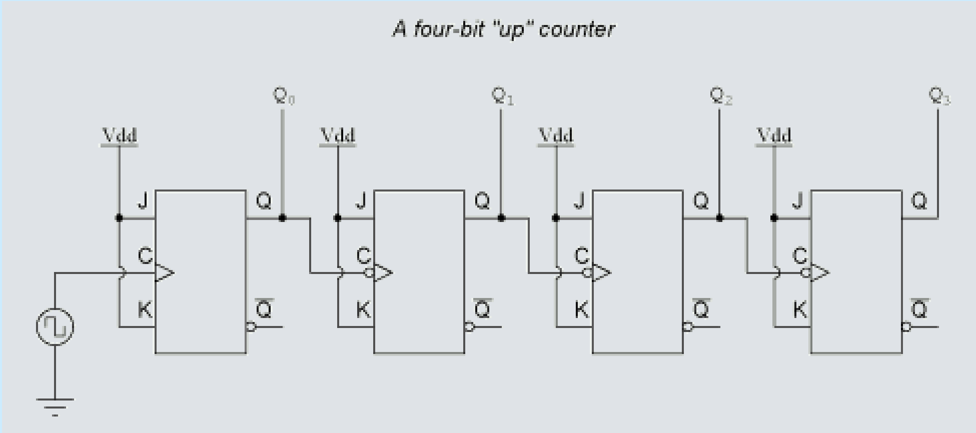
A different way of making a four-bit "up" counter
Vdd
J
C
K
Q
$\overline{Q}$
Q_0
Q_1
Q_2
Q_3

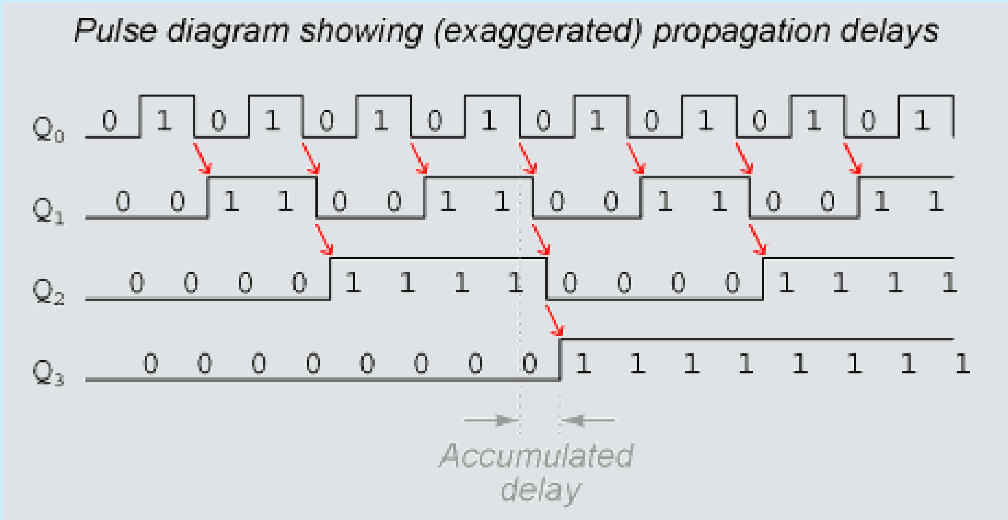
Up and Down counter

A simultaneous "up" and "down" counter

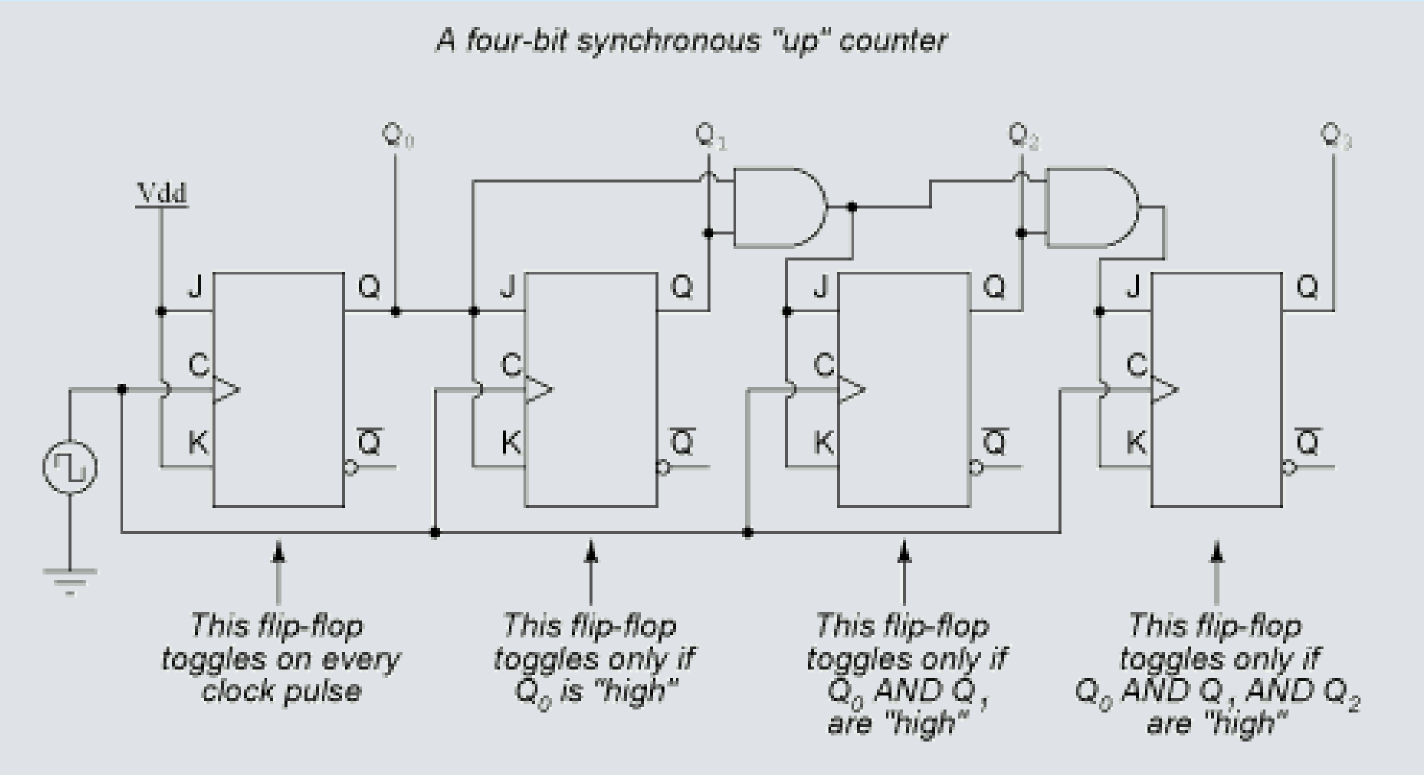


Propagation delay in asynchronous counter

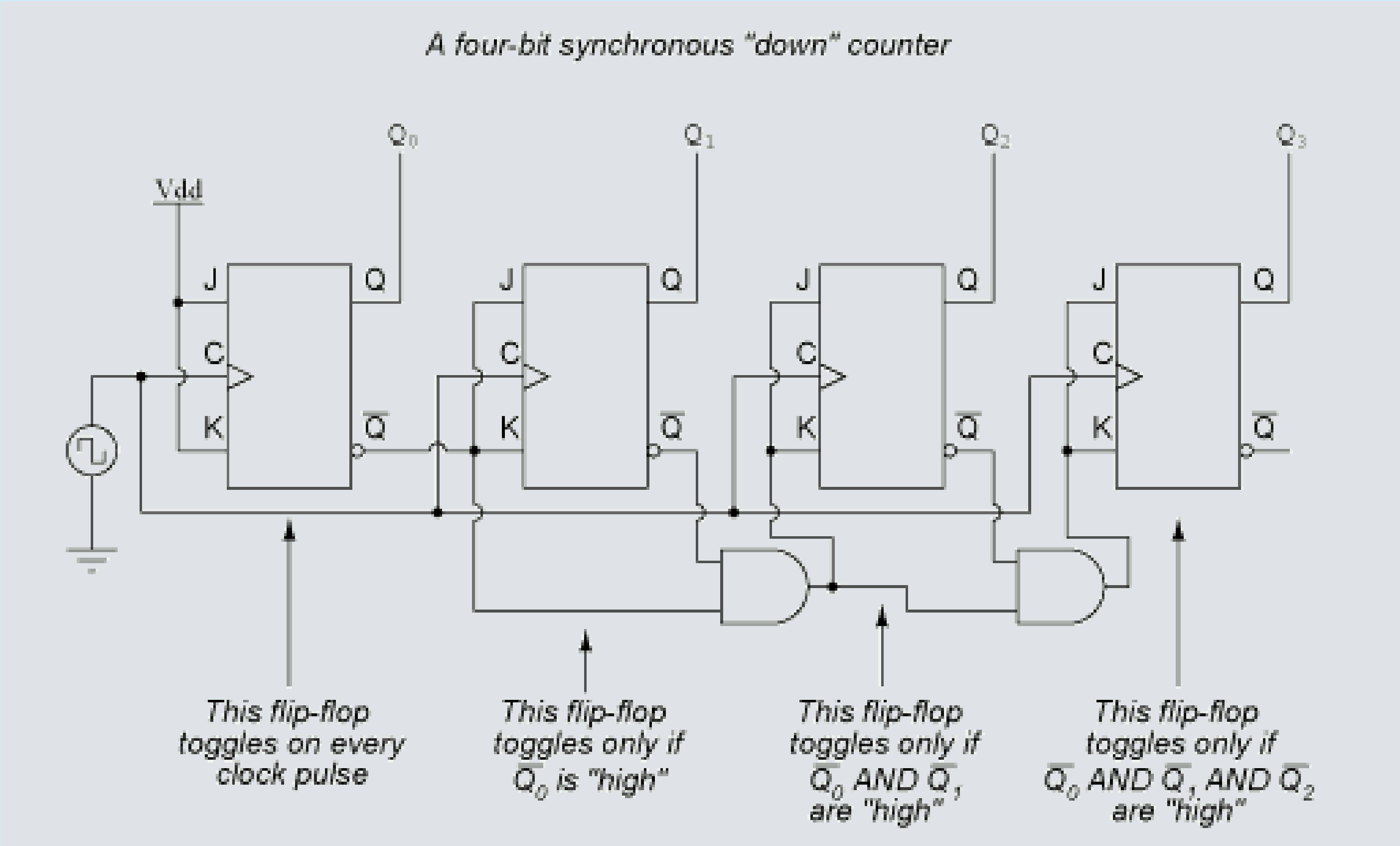




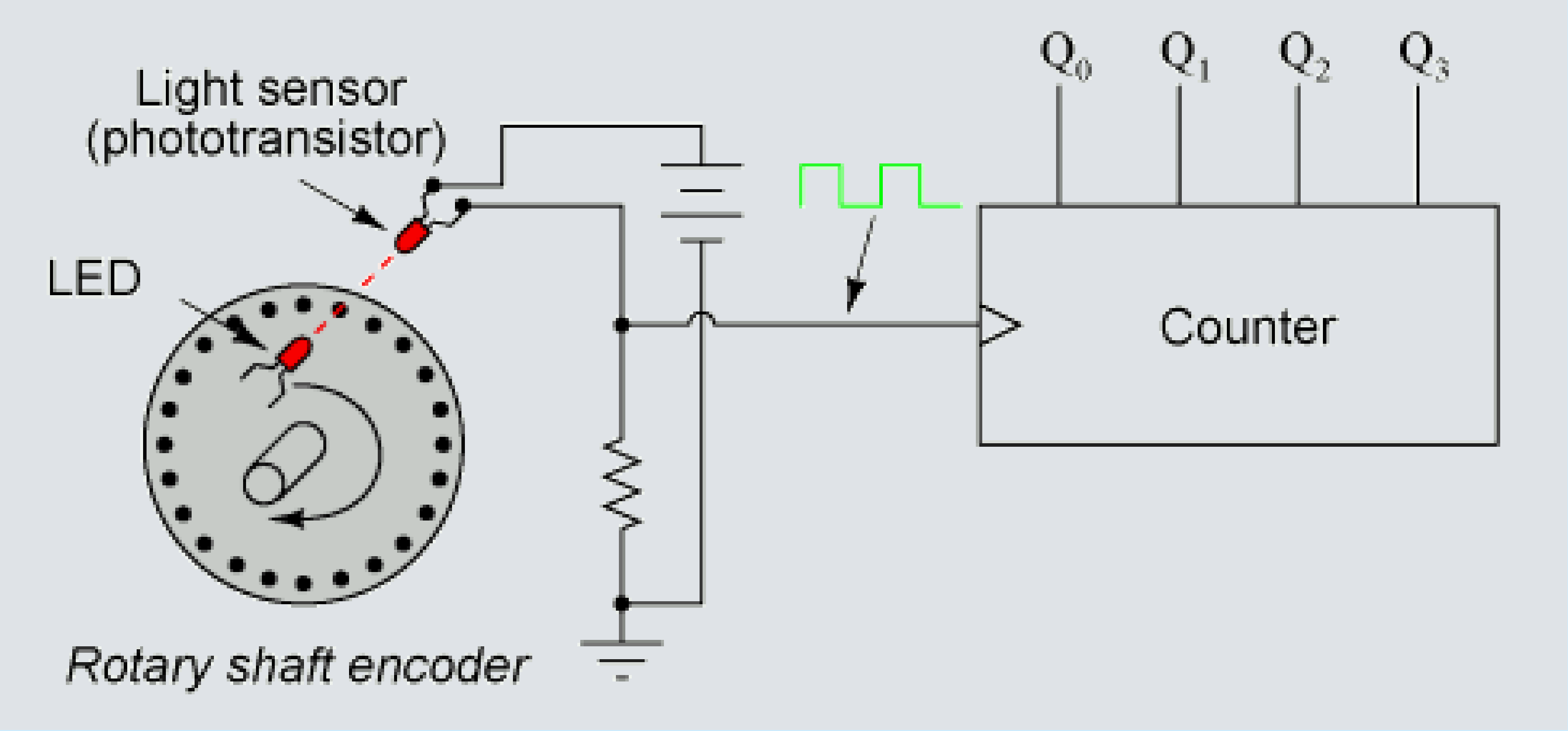
Synchronous counters



Contd.


A four-bit synchronous "down" counter
Q0
Q1
Q2
Q3
Vdd
J
C
K
Q
Q̄
This flip-flop toggles on every clock pulse
This flip-flop toggles only if Q̄0 is "high"
This flip-flop toggles only if Q̄0 AND Q̄1 are "high"
This flip-flop toggles only if Q̄0 AND Q̄1 AND Q̄2 are "high"

Application of counter



Problem

Application of counters ?

Shift Register

Application

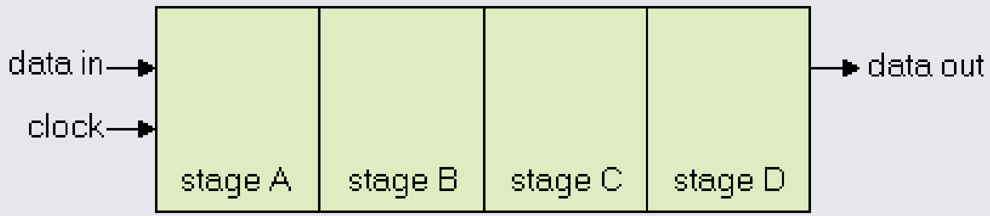
- Shift registers produce a discrete delay of a digital signal or waveform

- Very long shift registers served as digital memory

Shift Register Types

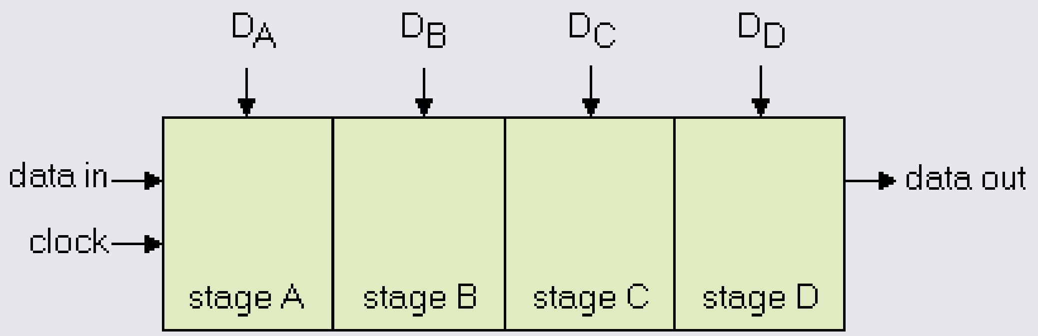
- Serial-in/serial-out
- Serial-in/parallel-out
- Parallel-in/serial-out
- Parallel-in/parallel-out
- Ring counter

Serial-in/serial-out



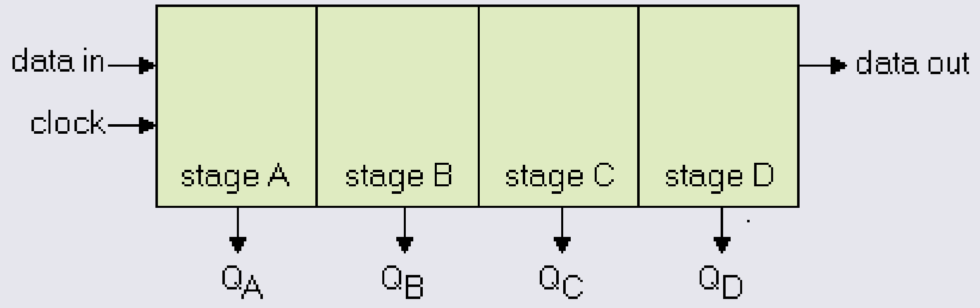
Serial-in, serial-out shift register with 4 stages

Parallel-in/serial-out



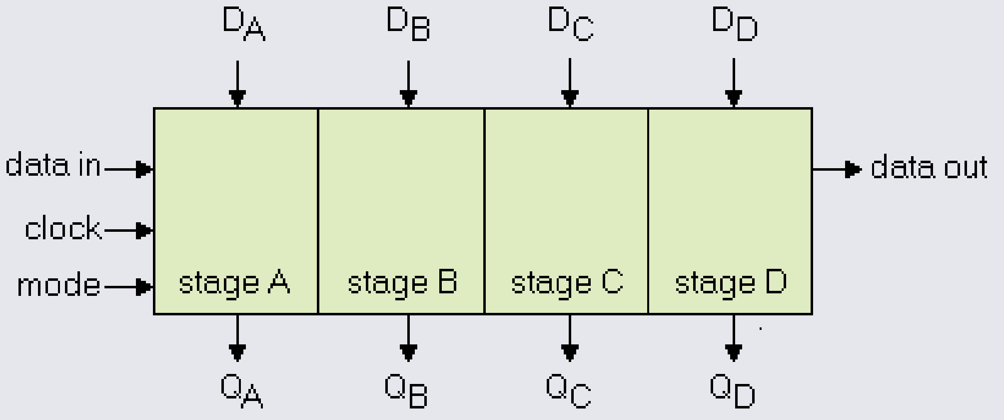
Parallel-in, serial-out shift register with 4 stages

Serial-in/parallel-out



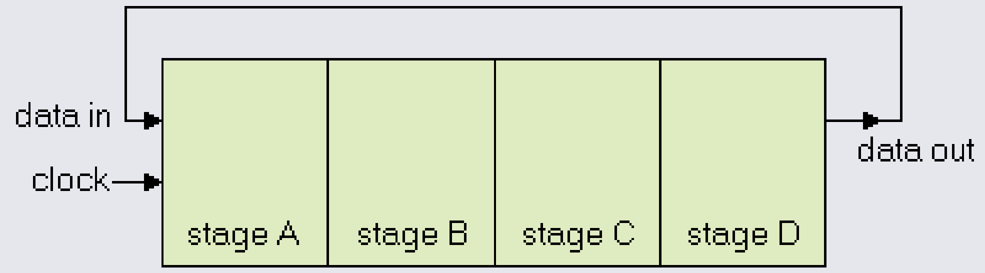
Serial-in, parallel-out shift register with 4 stages

Parallel-in/Parallel-out



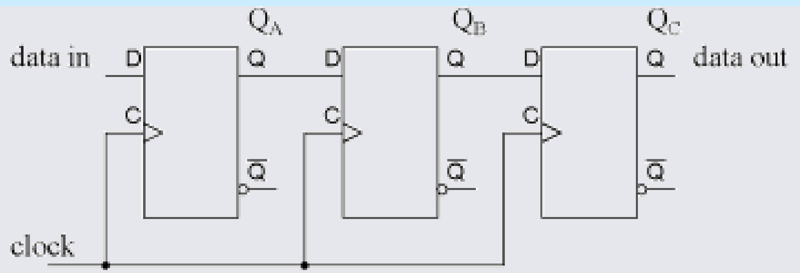
Parallel-in, parallel-out shift register with 4 stages

Ring counter

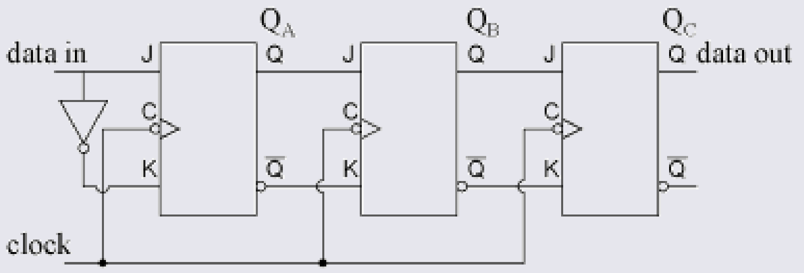


Ring Counter, shift register output fed back to the input

Serial-in, Serial-out shift register

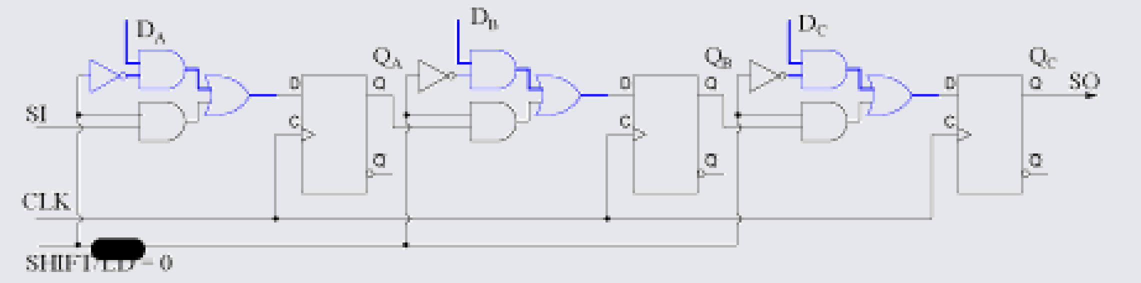


Serial-in, serial-out shift register using type "D" storage elements

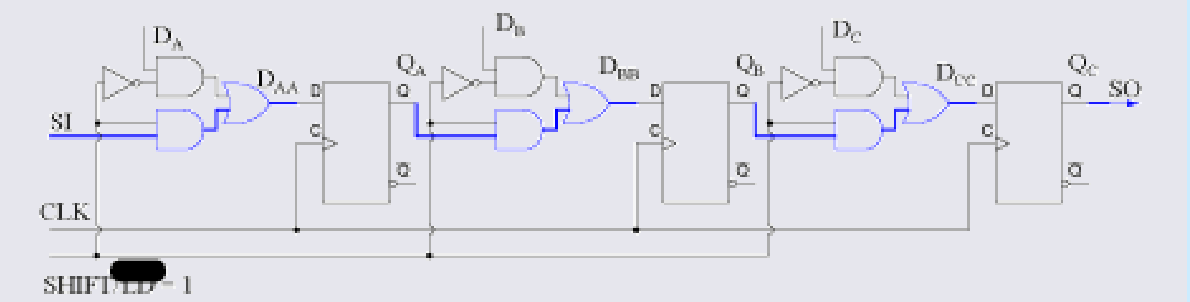


Serial-in, serial-out shift register using type "JK" storage elements

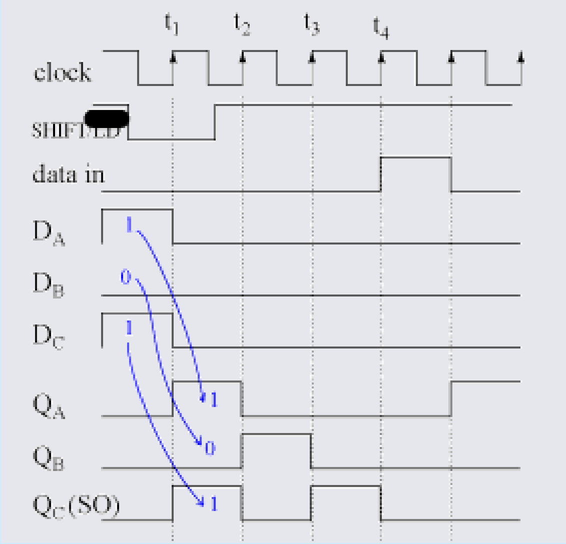
Parallel-in serial out



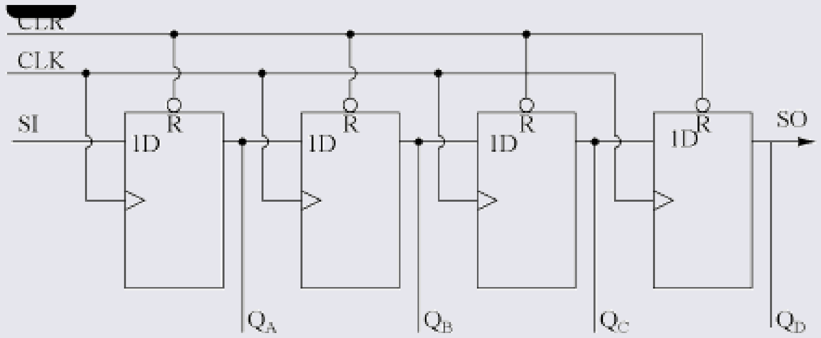
Parallel-in/ serial-out shift register showing parallel load path



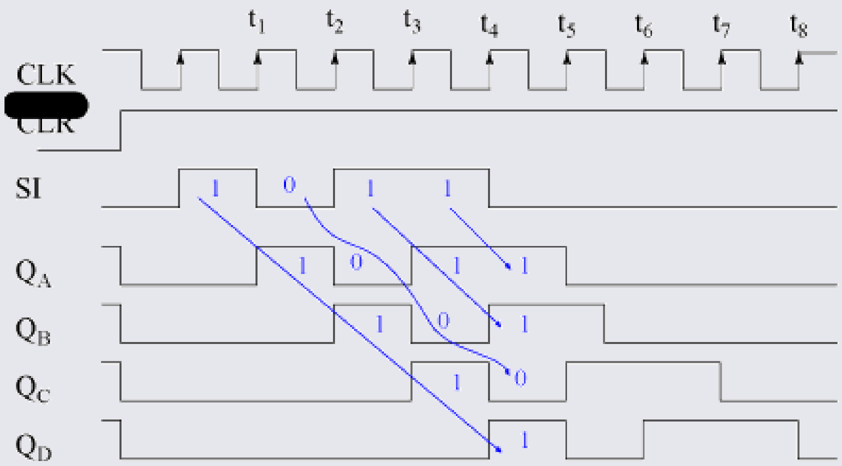
Parallel-in/ serial-out shift register showing shift path



Serial-in/parallel out



Serial-in/ Parallel out shift register details

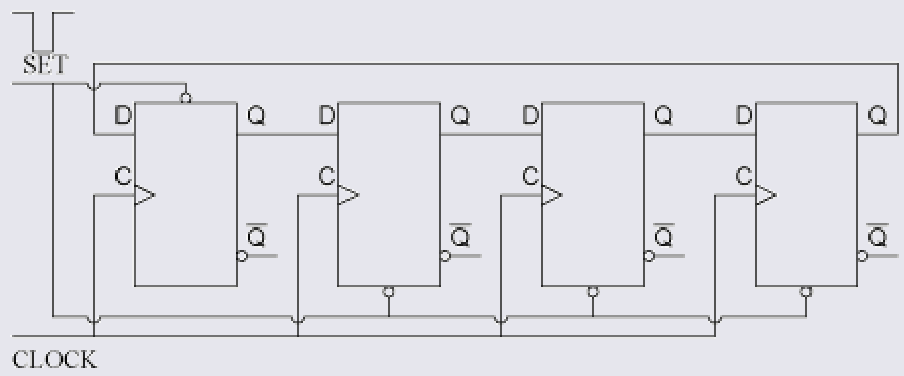


Serial-in/ parallel-out shift register waveforms

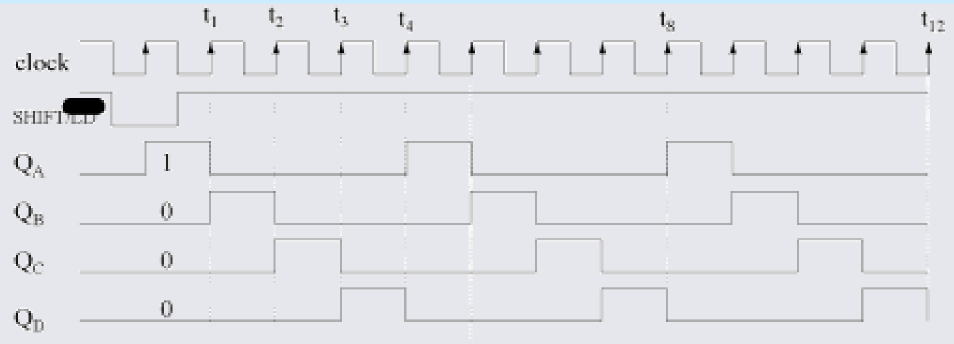
Problem

- Parallel-in parallel-out circuit ?

Ring counter



Set one stage, clear three stages



Load 1000 into 4-stage ring counter and shift

Digital Storage

Why digital ?

- The basic goal of digital memory is to provide a means to store binary data: sequences of 1's and 0's
- The most evident advantage of digital data storage is the resistance to corruption
  - Magnetization method of storage
- Digital data storage also complements digital computation technology

Random access and sequential access

- Random access means that you can quickly and precisely address a specific data location within the device, and non-random (sequential) simply means that you cannot
- Examples
  - A vinyl record platter is an example of a random-access device (CD's also)
  - Cassette tape is sequential

Writing and Reading

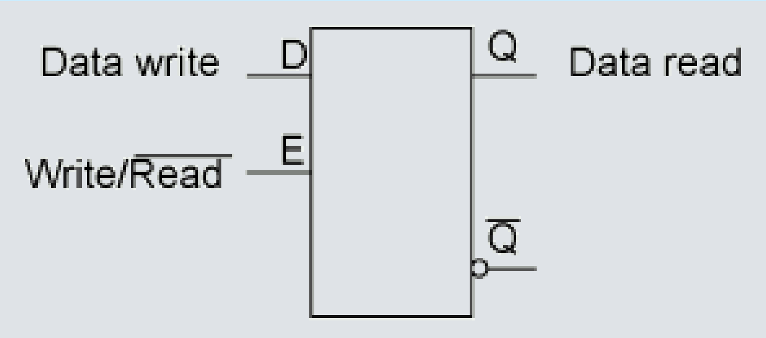
- The process of storing a piece of data to a memory device is called *writing*
- The process of retrieving data is called *reading*
- *ROM (read only memory)-* Some devices do not allow for the writing of new data, and are purchased "pre-written“.
  - Example: vinyl records
- *Read-write memory* – Memories allow reading and writing
  - Example: Cassette audio and video tape

Memory with moving parts: "Drives"

- Paper tape
- Magnetic tape (sequential access,slow)
- Magnetic storage drives drum type (motor, R/W coil)
- Floppy disk (not reliable)
- Hard drive
- Compact disk (CD)
  - Binary bits are "burned" into the aluminum as pits by a high-power laser
- Digital Video Disk (DVD)

Modern nonmechanical memory

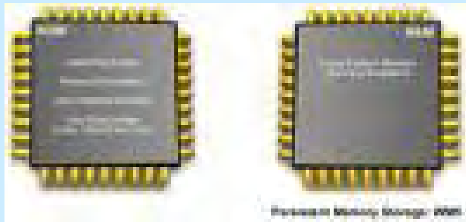
- A very simple type of electronic memory is flip-flop



ROM-Read-only memory

- PROMs - Programmable Read-Only Memory

  The simplest type of ROM is that which uses tiny "fuses" which can be selectively blown or left alone to represent the two binary states



- EPROM - Erasable Programmable Read-Only Memory
  - Electrically-erasable (EEPROM)
  - Ultraviolet-erasable (UV/EPROM)

Volatile and non-volatile memory

- Volatile memory loose its data when power goes off (e.g, RAM of computer)

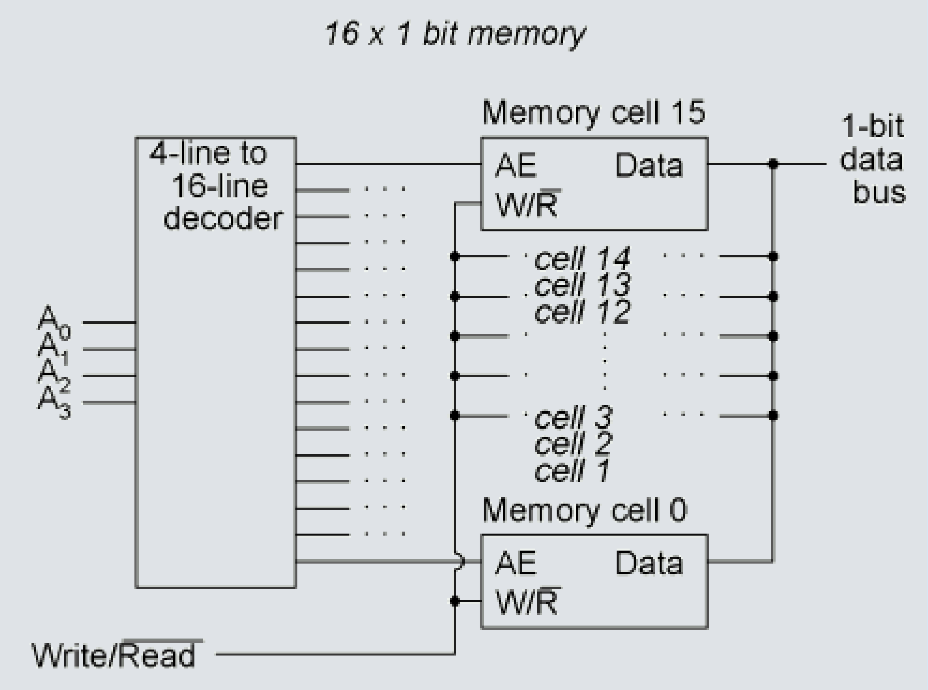
- Non Volatile memory retain data even without power (e.g. ROM, magnetic tapes)

Memory Address

- The location of this data within the storage device is typically called the *address*, in a manner reminiscent of the postal service.
  - the address in which certain data is stored can be called up by means of parallel data lines in a digital circuit
  - data is addressed in terms of an actual physical location on the surface of some type of media (e.g. *tracks* and *sectors* of circular computer disks)

Memory Array

For more storage, many latches arranged in a form of array where we can selectively address which one is reading from or writing to.



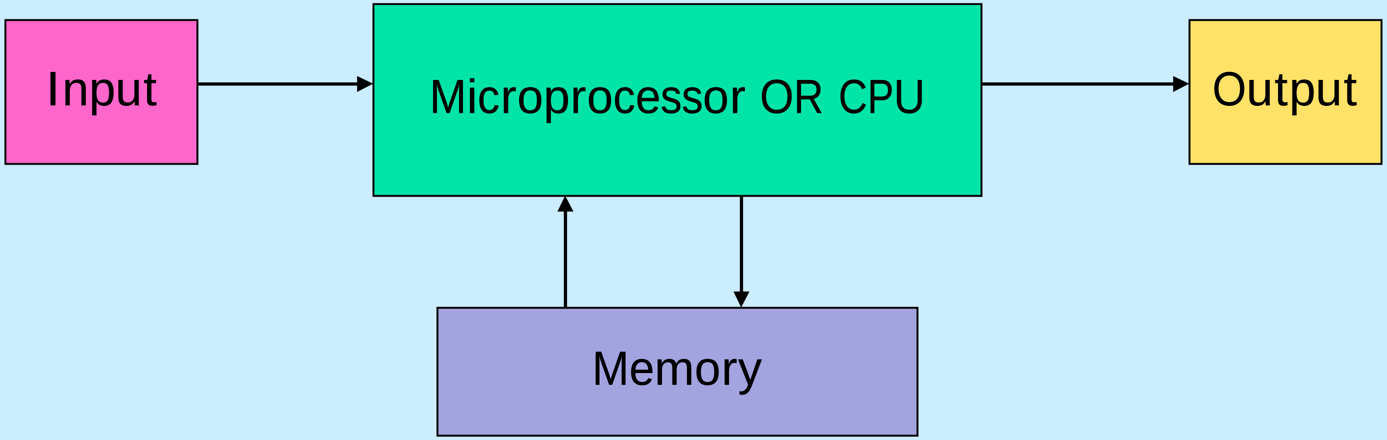
Memory Size

- Number of bits
- Generally memory size represented in bytes (1 byte = 8 bits)
  - Example
    - 1.6 Gigabytes = 12.8 Giga bits
  - “One kilobyte" = 1024 bytes (2 to the power of 10) locations for data bytes (rather than exactly 1000)
  - "64 kbyte" memory device actually holds 65,536 bytes of data (2 to the 16th power)

Digital computer

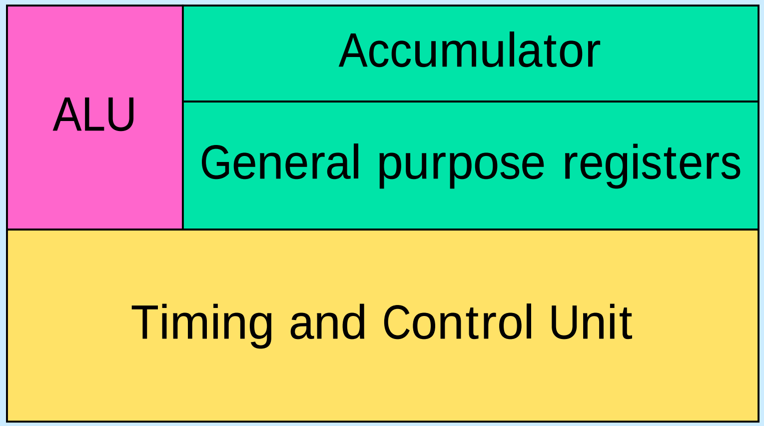
Main components

- CPU: central procession unit
- Memory
- Input output device



Microprocessor or CPU

- It fatches instruction from the memory and performs specified tasks.
- It store results in the memory or sends results to the output device
- It control with memory and input/output devices



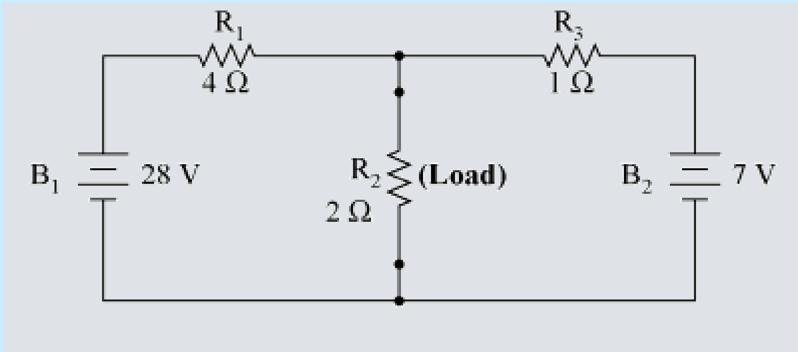
Sections of CPU

- Arithmetic and logic unit - to perform arithmetic operations such as addition and subtractions, logical operation (AND,OR, etc.)
- Timing and control unit - control entire operation of a computer. It acts as a brain. It also control all other devices connected to CPU
- General purpose registers - for temporary storage of data and intermediate results while computer is making execution of program
- Accumulator – It is a register which contain one the operands and store results of most arithmetic and logical operations

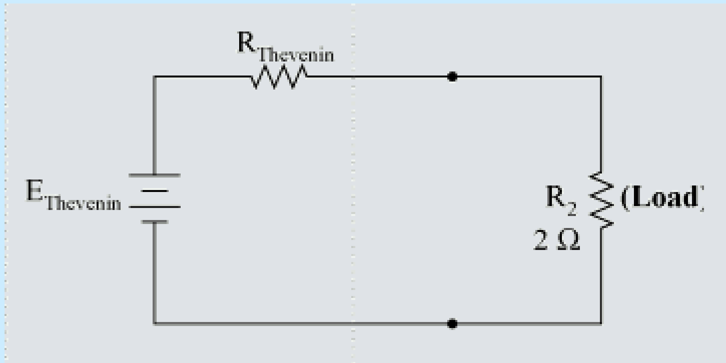
Electrical Theorem and Components

Thevenin's Theorem

- Thevenin's Theorem is a way to reduce a network to an equivalent circuit composed of a single voltage source, series resistance, and series load

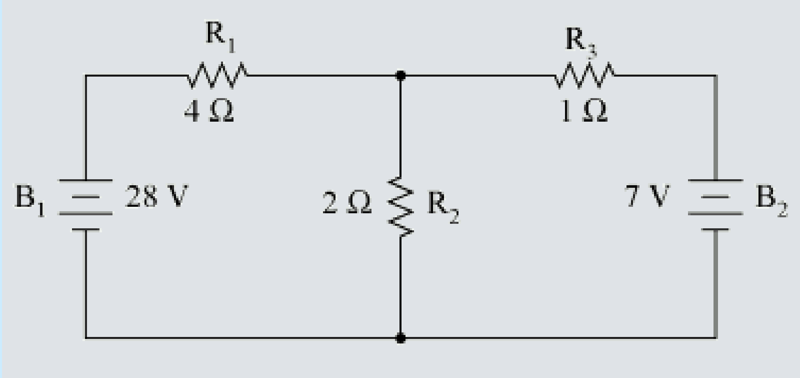


- Useful in analyzing power systems and other circuits where one particular resistor in the circuit (called the "load" resistor) is subject to change, and re-calculation of the circuit is necessary with each trial value of load resistance, to determine voltage across it and current through it.



Steps to follow for Thevenin's Theorem

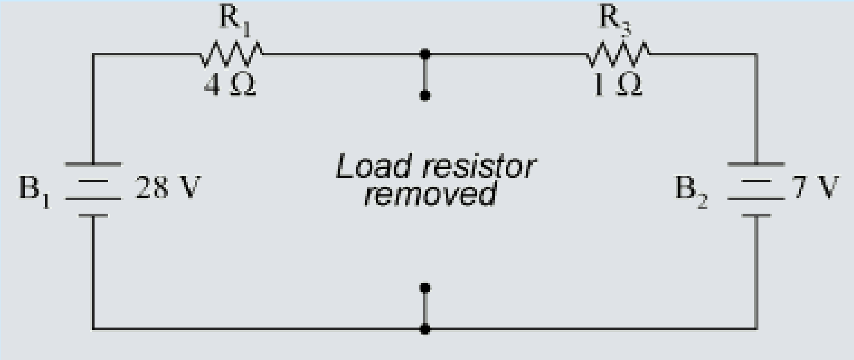
1. Find the Thevenin source voltage by removing the load resistor from the original circuit and calculating voltage across the open connection points where the load resistor used to be.



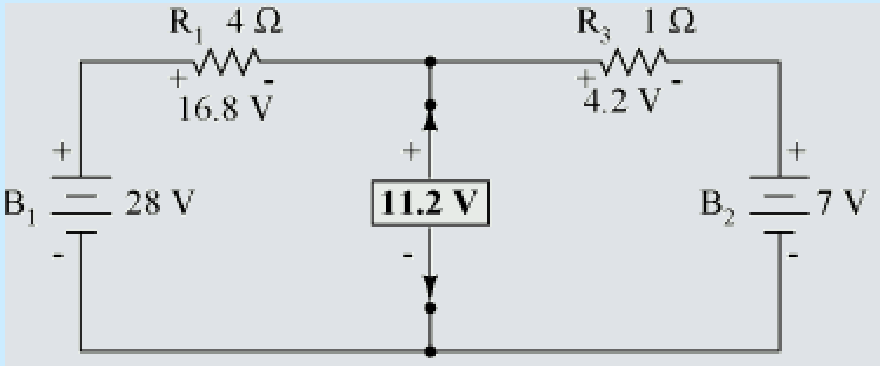
Designate R2 as the "load" resistor

Determining voltage and current across R2

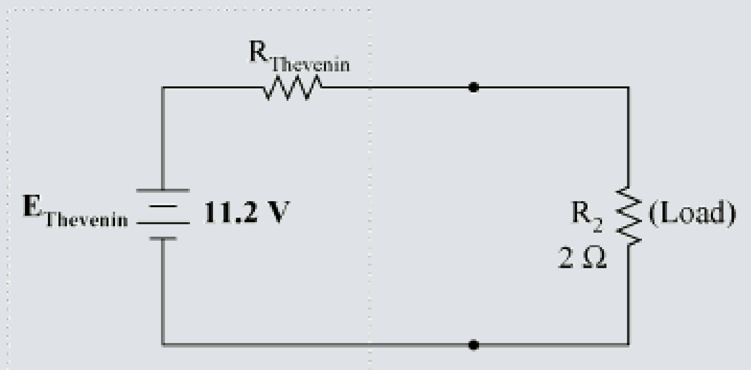
Contd.



	R_1	R_3	Total	
E	16.8	4.2	21	Volts
I	4.2	4.2	4.2	Amps
R	4	1	5	Ohms

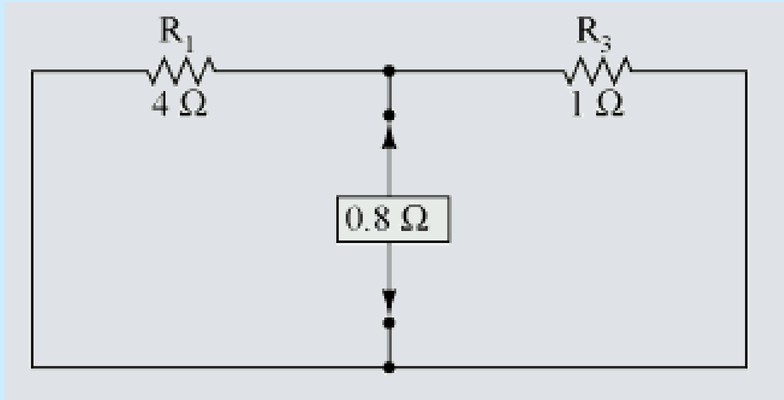


Thevenin Equivalent Circuit



Contd.

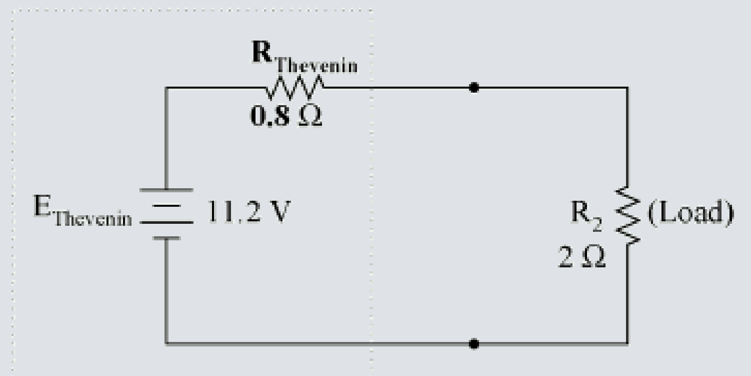
2. Find the Thevenin resistance by removing all power sources in the original circuit (voltage sources shorted and current sources open) and calculating total resistance between the open connection points.



Contd.

3. Draw the Thevenin equivalent circuit, with the Thevenin voltage source in series with the Thevenin resistance. The load resistor re-attaches between the two open points of the equivalent circuit.
4. Analyze voltage and current for the load resistor following the rules for series circuits.

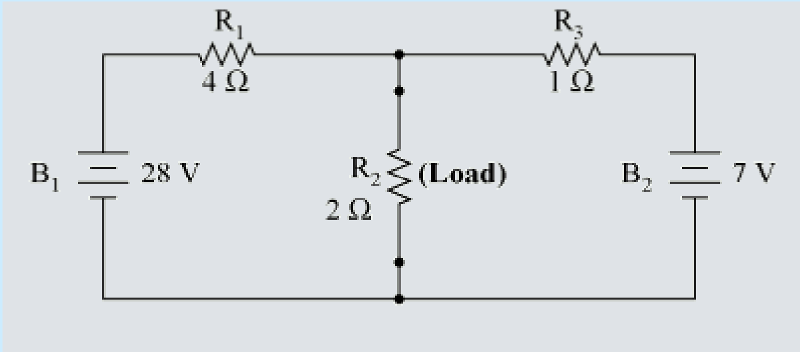
Thevenin Equivalent Circuit

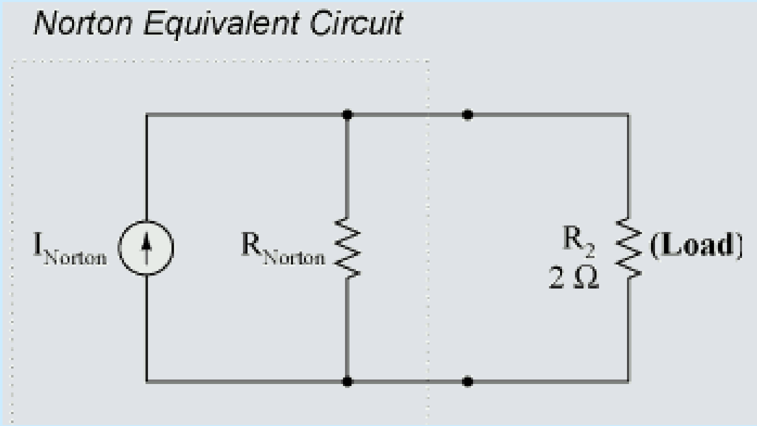


	$R_{Thevenin}$	R_{Load}	Total	
E	3.2	8	11.2	Volts
I	4	4	4	Amps
R	0.8	2	2.8	Ohms

Norton's Theorem

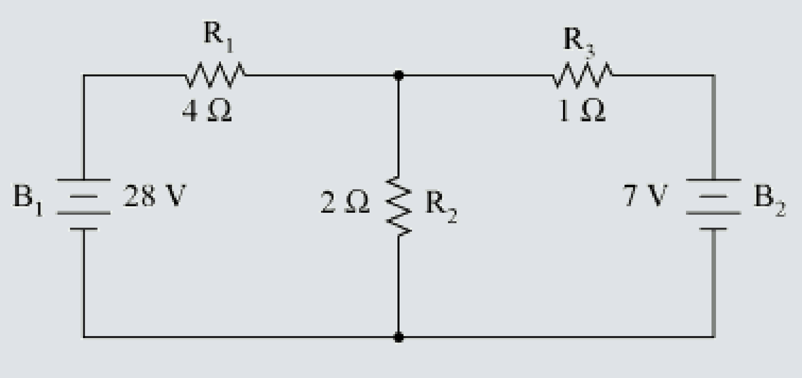
- Norton's Theorem is a way to reduce a network to an equivalent circuit composed of a single current source, parallel resistance, and parallel load.
- Useful in analyzing power systems and other circuits where one particular resistor in the circuit (called the "load" resistor) is subject to change, and re-calculation of the circuit is necessary with each trial value of load resistance, to determine voltage across it and current through it.





Steps to follow for Norton's Theorem

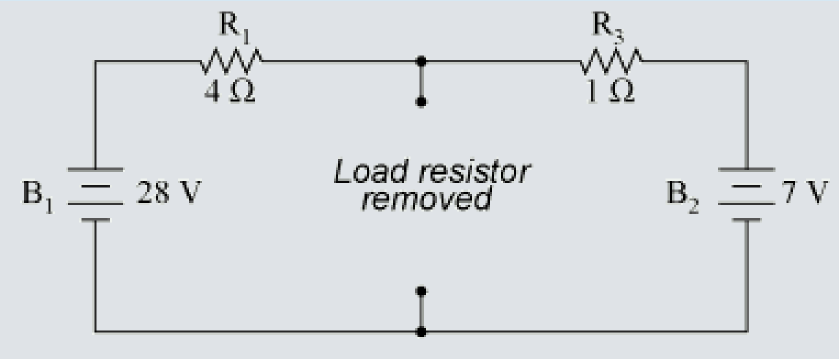
1. Find the Norton source current by removing the load resistor from the original circuit and calculating current through a short (wire) jumping across the open connection points where the load resistor used to be



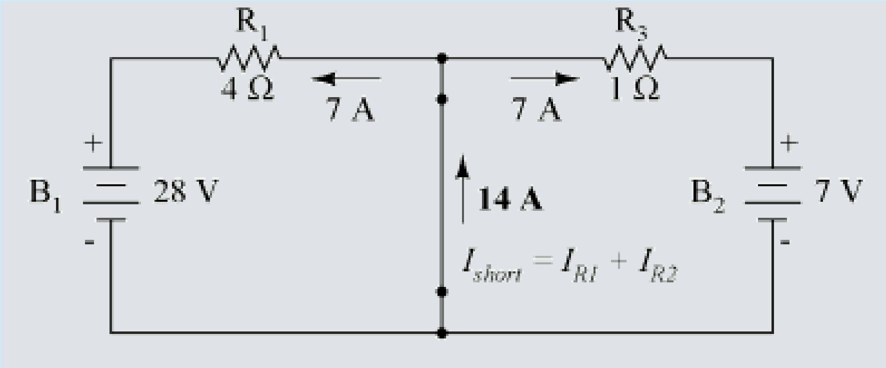
Designate R2 as the "load" resistor

Determining voltage and current across R2

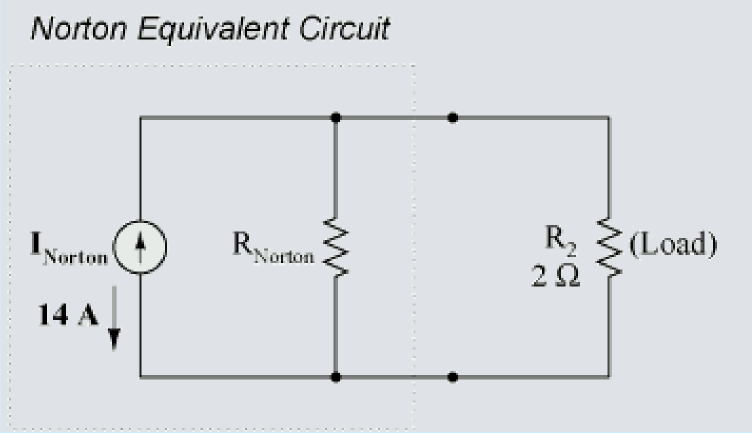
Contd.



R1
4 Ω
R3
1 Ω
B1
28 V
Load resistor removed
B2
7 V



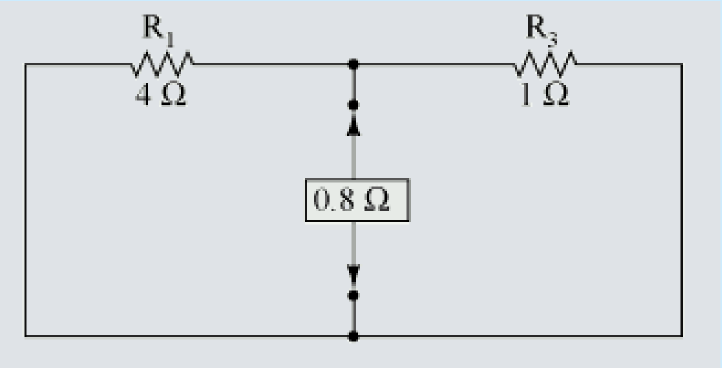
R1
4 Ω
7 A
R3
1 Ω
7 A
+
B1
28 V
-
14 A
$I_{short} = I_{R1} + I_{R2}$
+
B2
7 V
-



Norton Equivalent Circuit
I_{Norton}
14 A
R_{Norton}
R2
2 Ω
(Load)

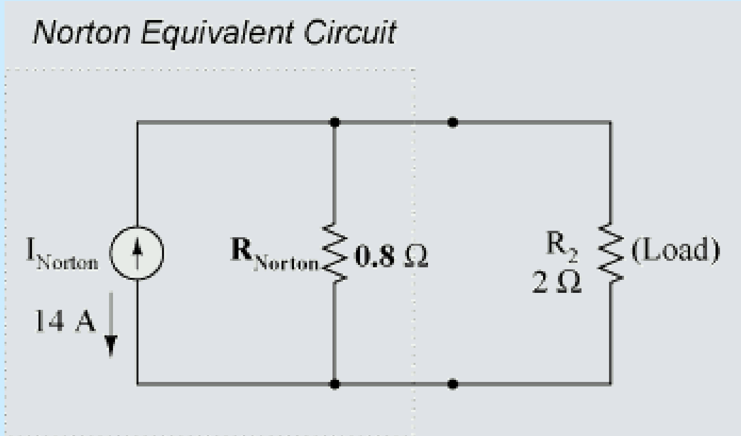
Contd.

2. Find the Norton resistance by removing all power sources in the original circuit (voltage sources shorted and current sources open) and calculating total resistance between the open connection points.



Contd.

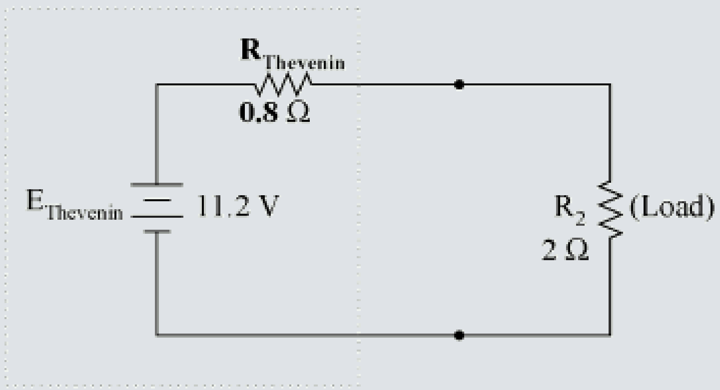
3. Draw the Norton equivalent circuit, with the Norton current source in parallel with the Norton resistance. The load resistor re-attaches between the two open points of the equivalent circuit.
4. Analyze voltage and current for the load resistor following the rules for parallel circuits.



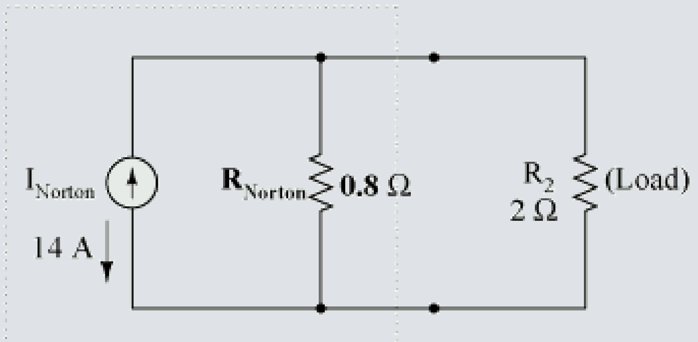
	R_{Norton}	R_{Load}	Total	
E	8	8	8	Volts
I	10	4	14	Amps
R	0.8	2	571.43m	Ohms

Thevenin-Norton equivalencies

Thevenin Equivalent Circuit



Norton Equivalent Circuit



$$R_{Thevenin} = R_{Norton}$$

$$E_{Thevenin} = I_{Norton} R_{Norton}$$

$$I_{Norton} = \frac{E_{Thevenin}}{R_{Thevenin}}$$

Electrical Components

Capacitor

- The ability of a capacitor to store energy in the form of an electric field is called *capacitance*. It is measured in the unit of the *Farad* (F).
- Capacitors used to be commonly known by another term: *condenser.*
- Capacitors react against changes in voltage.
- When a capacitor is faced with an increasing voltage, it acts as a *load*: drawing current as it absorbs energy.
- When a capacitor is faced with a decreasing voltage, it acts as a *source*: supplying current as it releases stored energy.

Capacitors and calculus

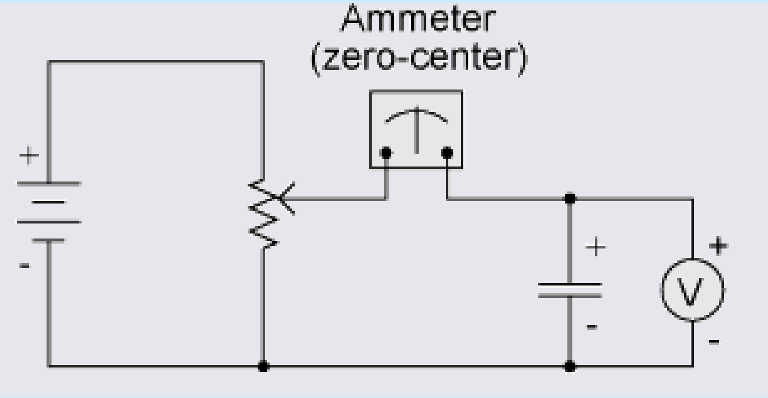
$$i = C\frac{dv}{dt}$$

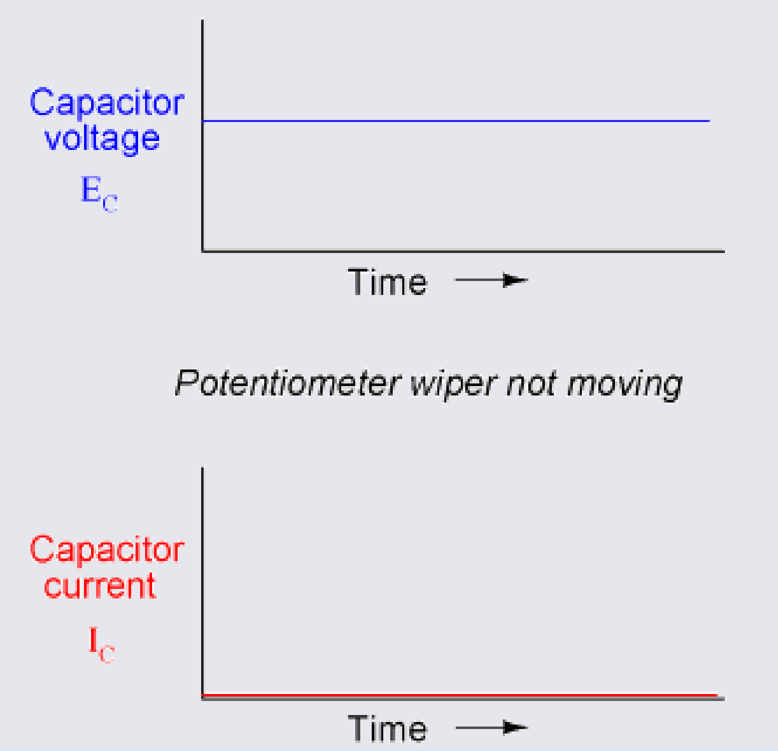
Where,

i = Instantaneous current through the capacitor

C = Capacitance in Farads

$\frac{dv}{dt}$ = Instantaneous rate of voltage change (volts per second)





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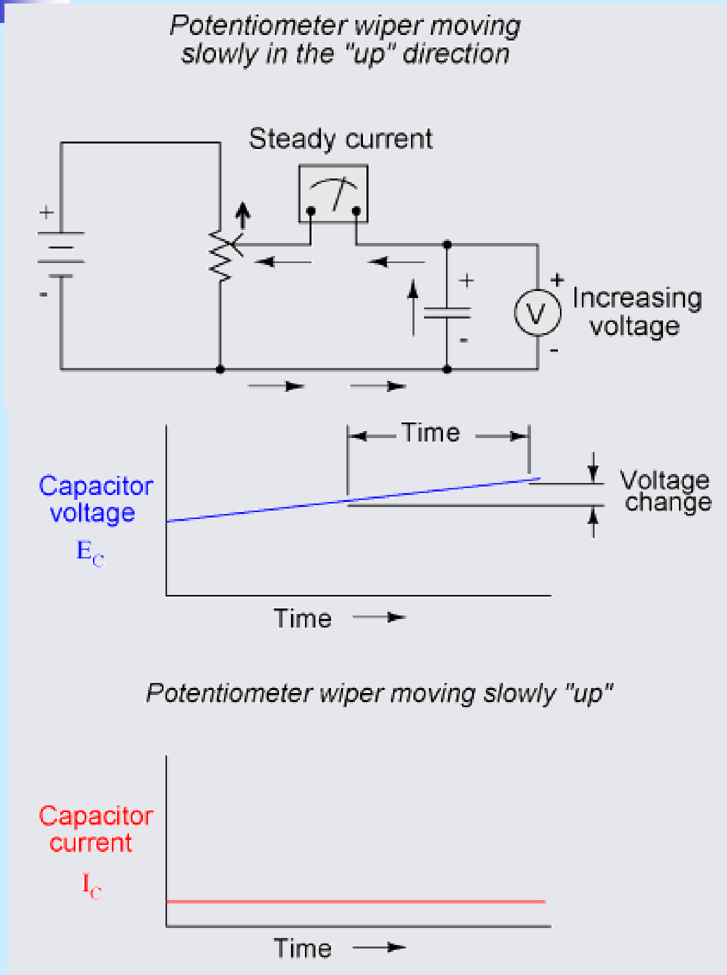
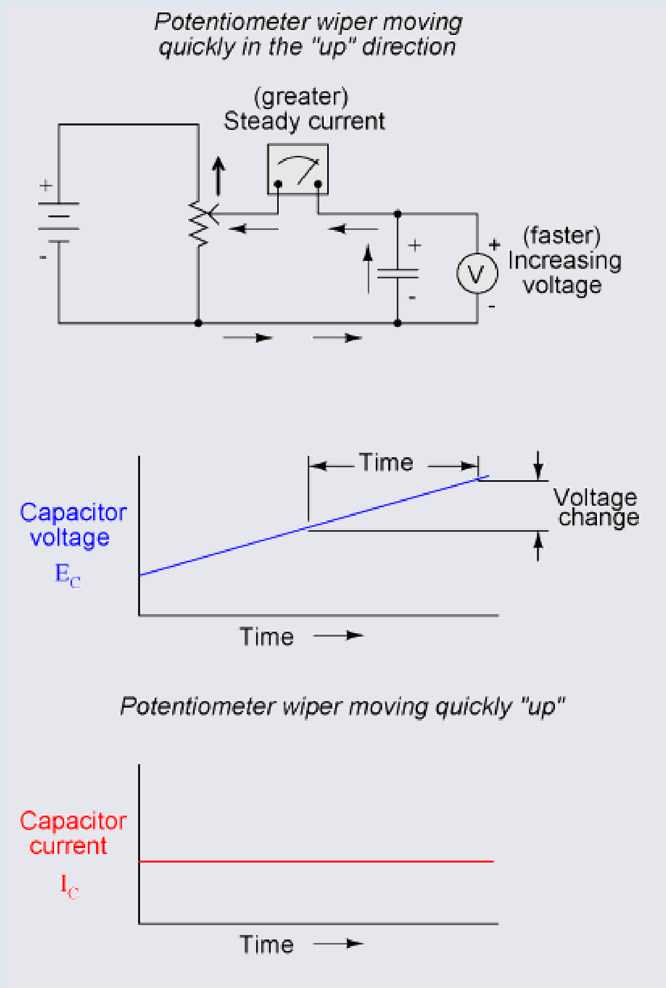
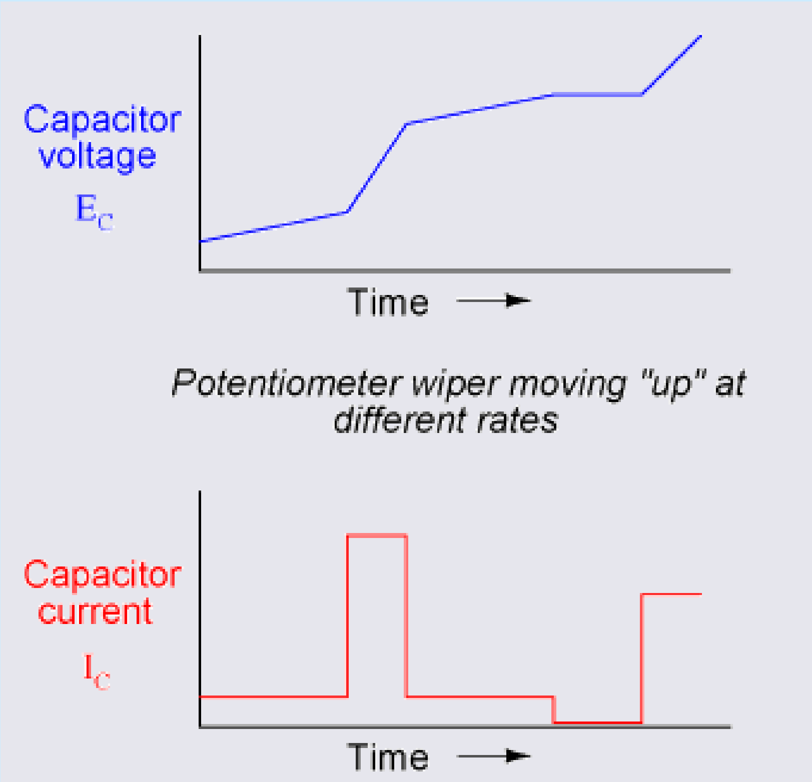
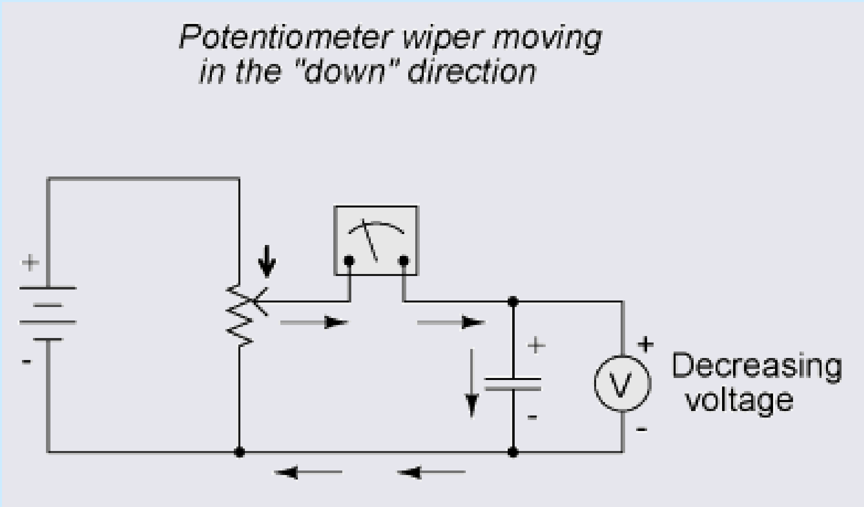

Potentiometer wiper moving
slowly in the "up" direction
Steady current
Increasing
voltage
Capacitor
voltage
E_C
Time
Voltage
change
Time
Potentiometer wiper moving slowly "up"
Capacitor
current
I_C
Time


Potentiometer wiper moving
quickly in the "up" direction
(greater)
Steady current
(faster)
Increasing
voltage
Capacitor
voltage
E_C
Time
Voltage
change
Time
Potentiometer wiper moving quickly "up"
Capacitor
current
I_C
Time

Contd.


Capacitor voltage
E_C
Time
Potentiometer wiper moving "up" at different rates
Capacitor current
I_C
Time


Potentiometer wiper moving in the "down" direction
+
-
+
-
V
+
-
Decreasing voltage

Factors affecting capacitance

$$C = \frac{\varepsilon A}{d}$$

Where,

$C =$ Capacitance in Farads

$\varepsilon =$ Permittivity of dielectric (absolute, not relative)

$A =$ Area of plate overlap in square meters

$d =$ Distance between plates in meters

- PLATE AREA
- PLATE SPACING
- DIELECTRIC MATERIAL

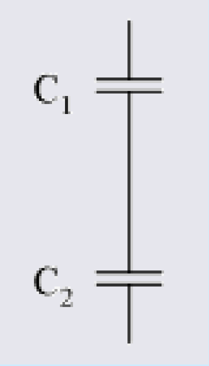
Series and parallel capacitors

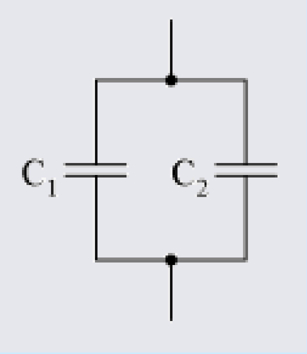
Series Capacitances

$$C_{total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \ldots \frac{1}{C_n}}$$

Parallel Capacitances

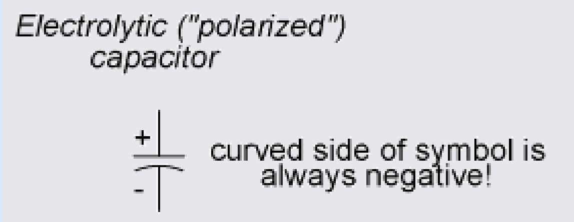
$$C_{total} = C_1 + C_2 + \ldots C_n$$

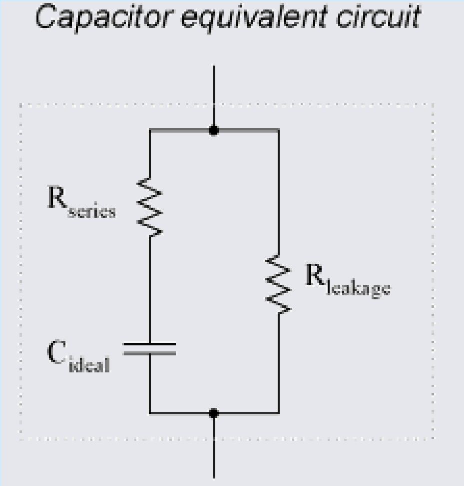


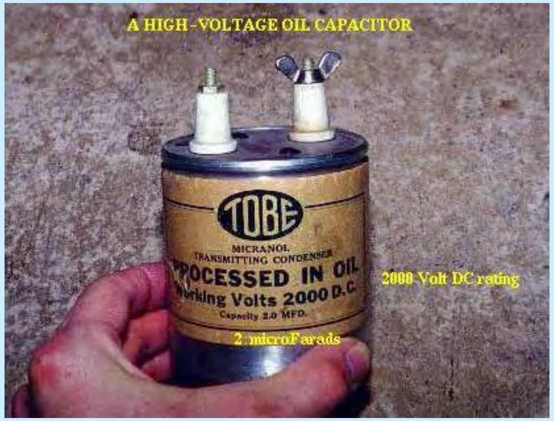


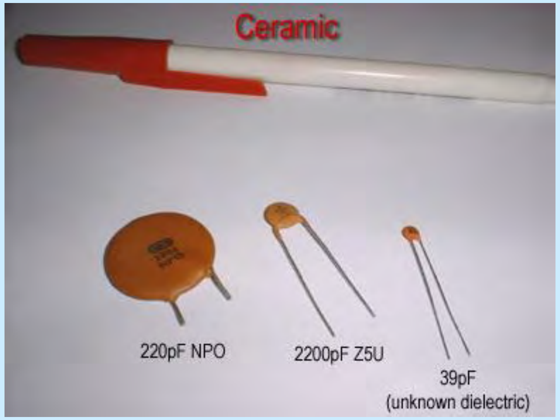
Practical considerations

- Working voltage
- Polarity
- Equivalent circuit
- Physical Size









Inductors

- The ability of an inductor to store energy in the form of a magnetic field is called *inductance*. It is measured in the unit of the *Henry* (H).
- Inductors used to be commonly known by another term: *choke*. In large power applications, they are sometimes referred to as *reactors*.
- Inductors react against changes in current by dropping voltage in the polarity necessary to oppose the change.
- When an inductor is faced with an increasing current, it acts as a load
- When an inductor is faced with a decreasing current, it acts as a source

Inductors and calculus

"Ohm's Law" for an inductor

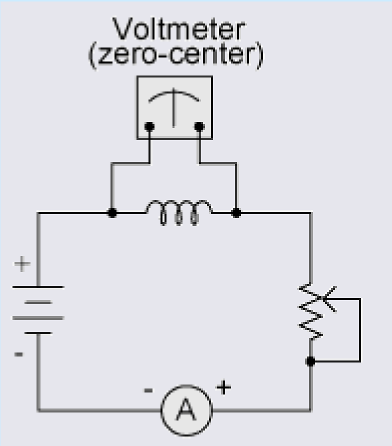
$$v = L\frac{di}{dt}$$

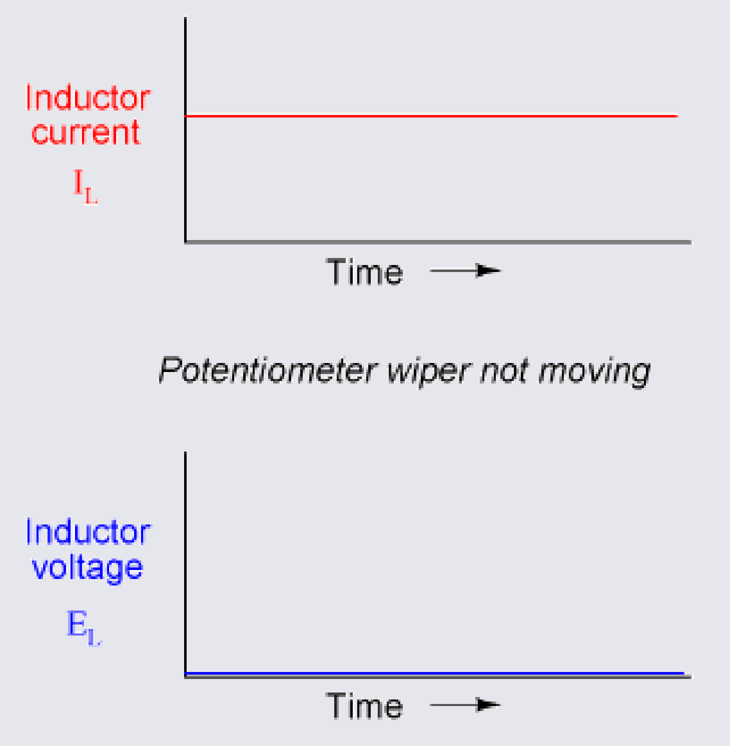
Where,

v = Instantaneous voltage across the inductor

L = Inductance in Henrys

$\frac{di}{dt}$ = Instantaneous rate of current change (amps per second)





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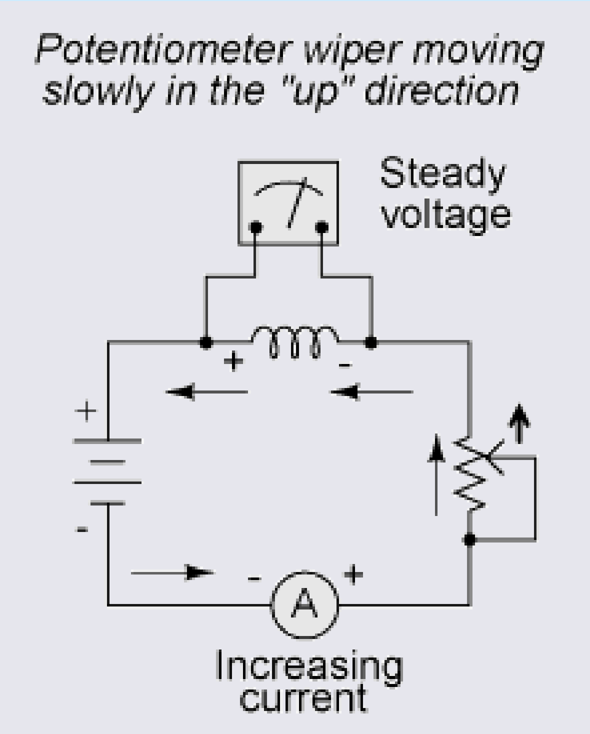
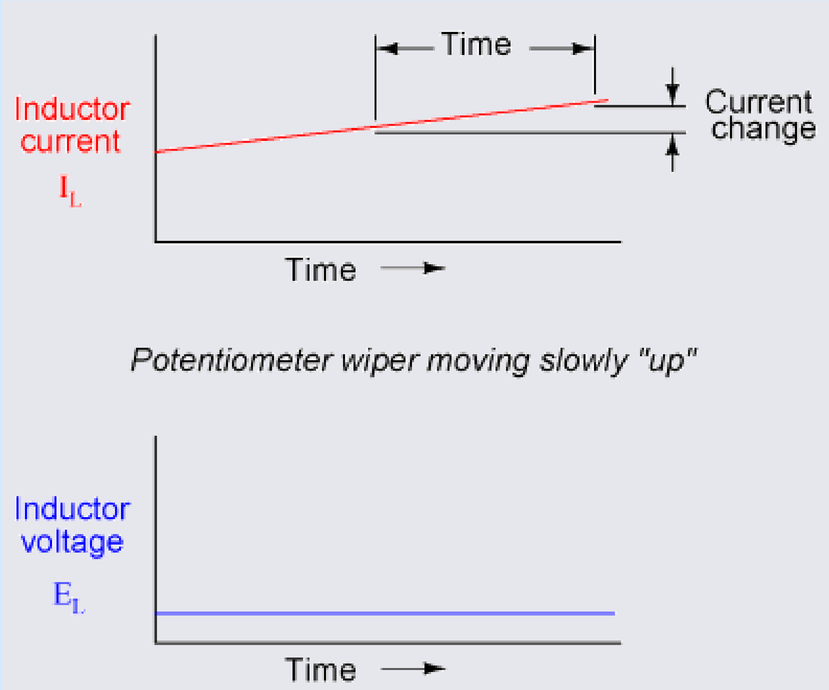
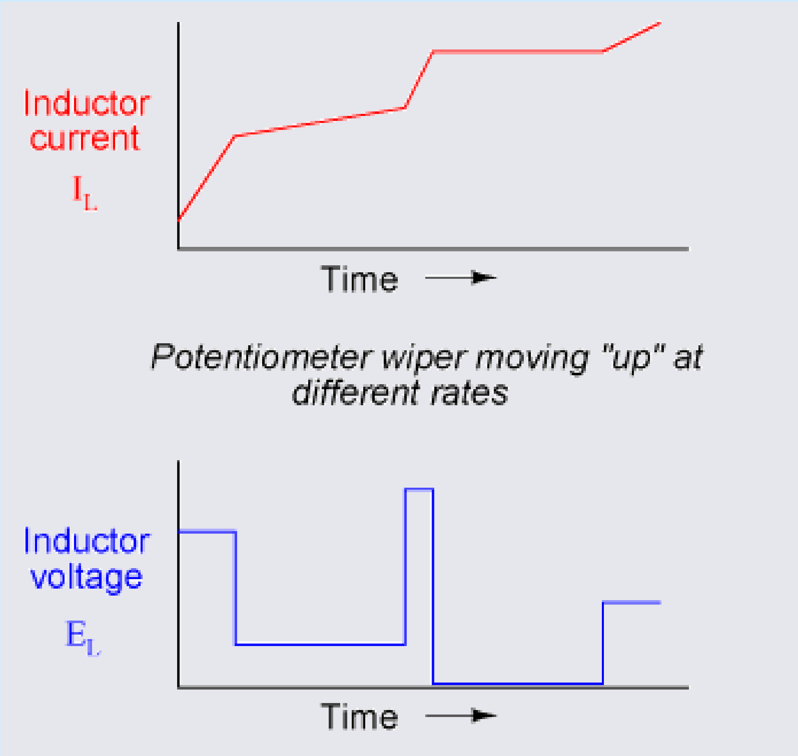


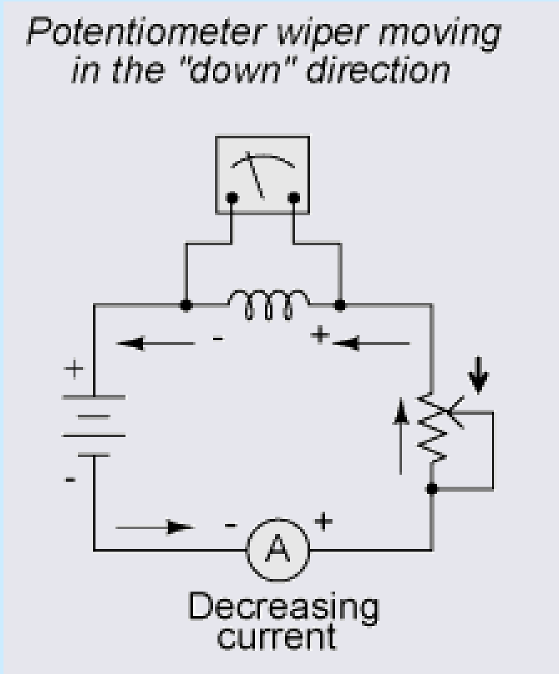
Potentiometer wiper moving slowly in the "up" direction
Steady voltage
+
-
+
-
-
+
A
Increasing current



Time
Inductor current
I_L
Current change
Time
Potentiometer wiper moving slowly "up"
Inductor voltage
E_L
Time

Contd.


Inductor current
I_L
Time
Potentiometer wiper moving "up" at different rates
Inductor voltage
E_L
Time


Potentiometer wiper moving in the "down" direction
-
+
+
-
-
+
A
Decreasing current

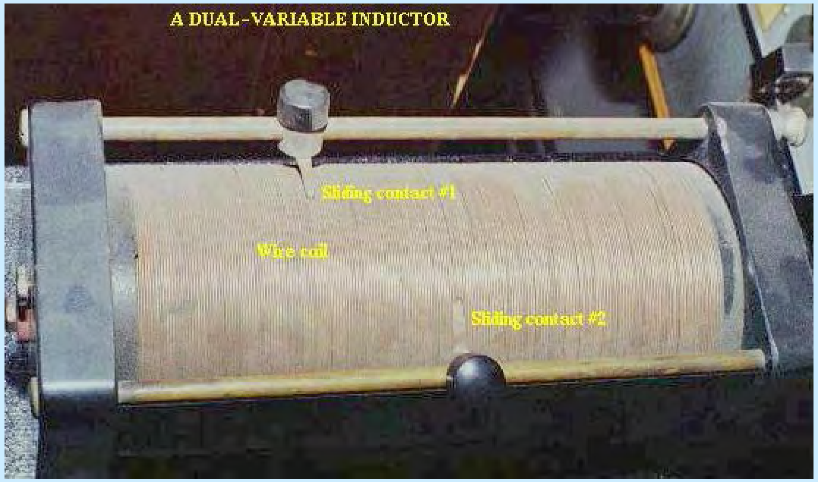
Factors affecting inductance

$$L = \frac{N^2 \mu A}{l}$$

Where,

L = Inductance of coil in Henrys
N = Number of turns in wire coil (straight wire = 1)
μ = Permeability of core material (absolute, not relative)
A = Area of coil in square meters
l = Average length of coil in meters

- TURNS IN THE COIL
- COIL AREA
- COIL LENGTH
- CORE MATERIAL



Series and parallel inductors

Series Inductances

$$L_{total} = L_1 + L_2 + \ldots L_n$$

Parallel Inductances

$$L_{total} = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots \frac{1}{L_n}}$$

Practical considerations

- Rated current
- Equivalent circuit
- Inductor size
- Interference

Analog Electronics

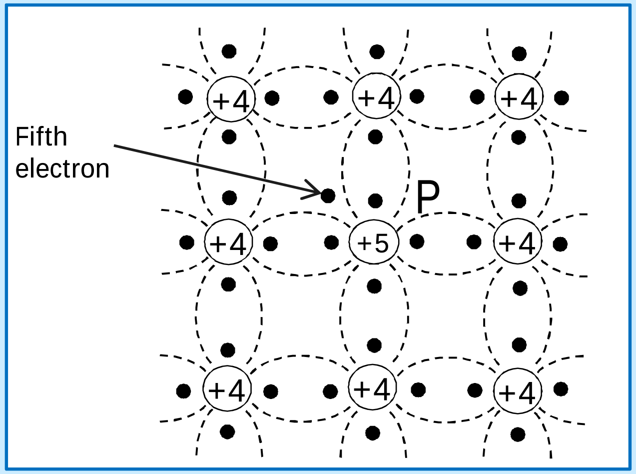
References

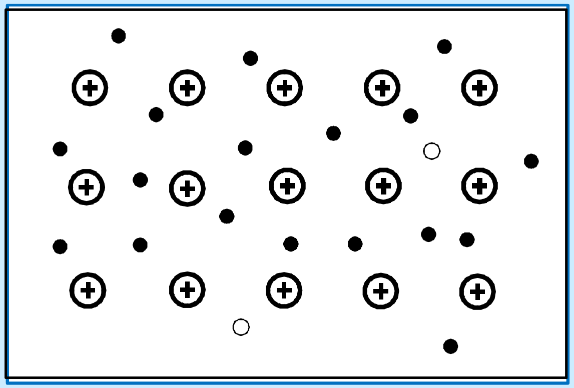
- A.P. **Malvino, Eletronic Principles**, Tata McGraw-Hill Publishing Company Limited, New Delhi

- N.N. **Bhargava**, D.C. Kulshreshtha, S.C. Gupta, **Basic Electronics and Linear Circuits**, Tata McGraw-Hill Publishing Company Limited, New Delhi

Diodes

n-type semiconductor

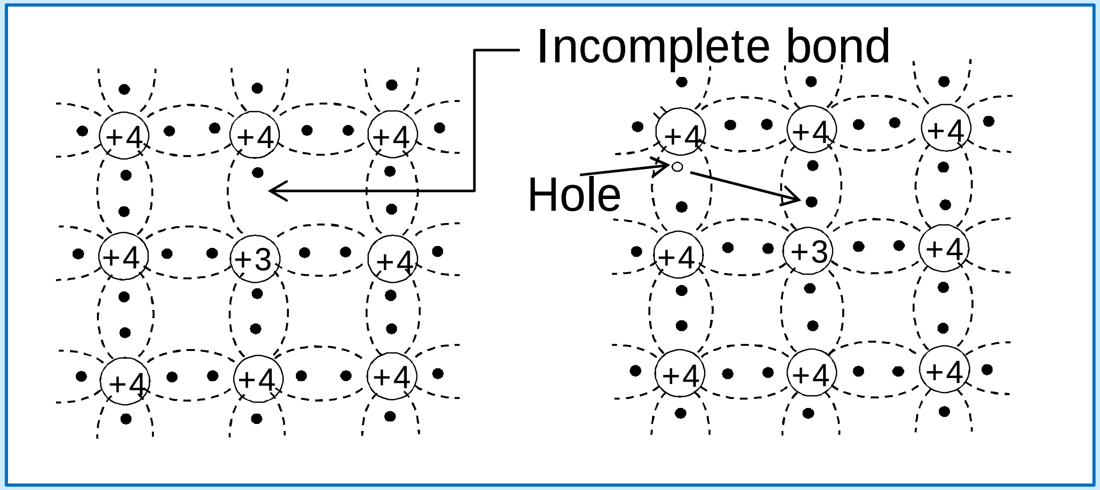


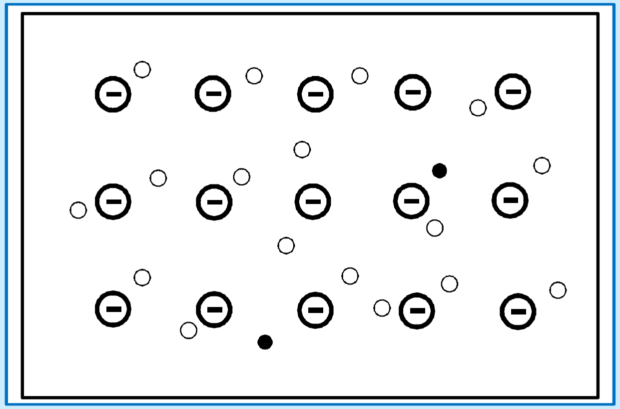


Legends :

- Free electron (Negative Charge)
- ○ Hole (Positive Charge)
- ⊕ Immobile ion (Positive Charge)

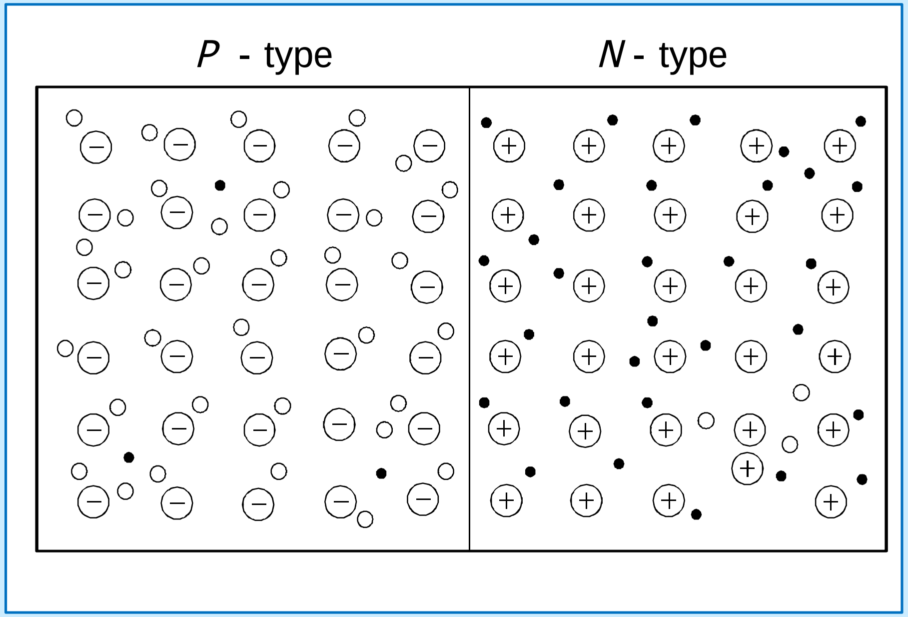
p-type semiconductor

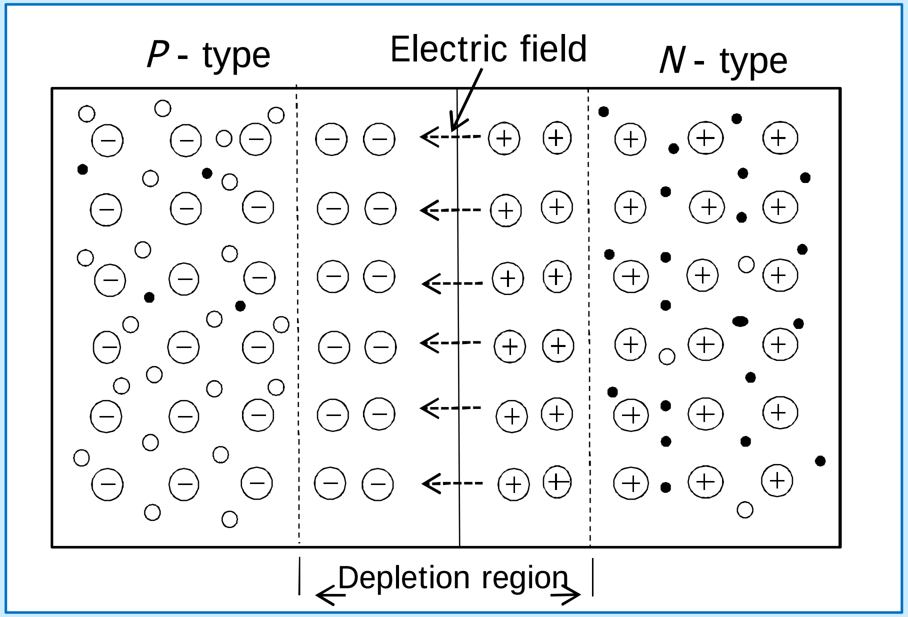




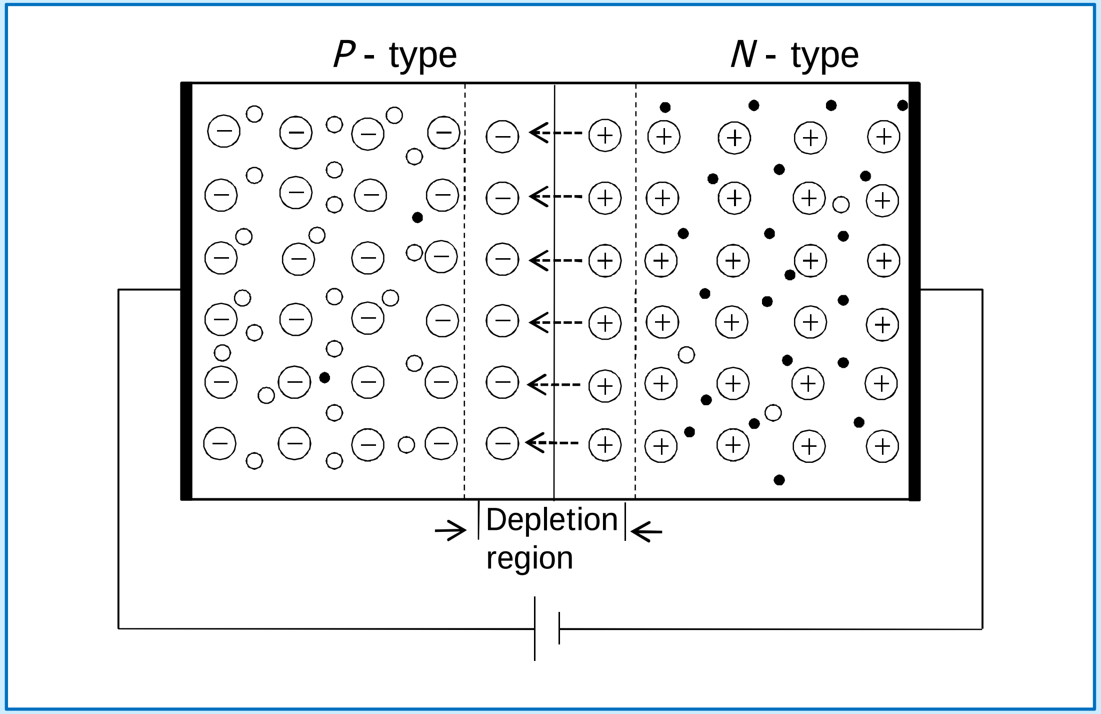
Legends :
- ○ Hole (Positive Charge)
- • Electron (Negative Charge)
- ⊖ Immobile ion (Negative Charge)

p-n junction

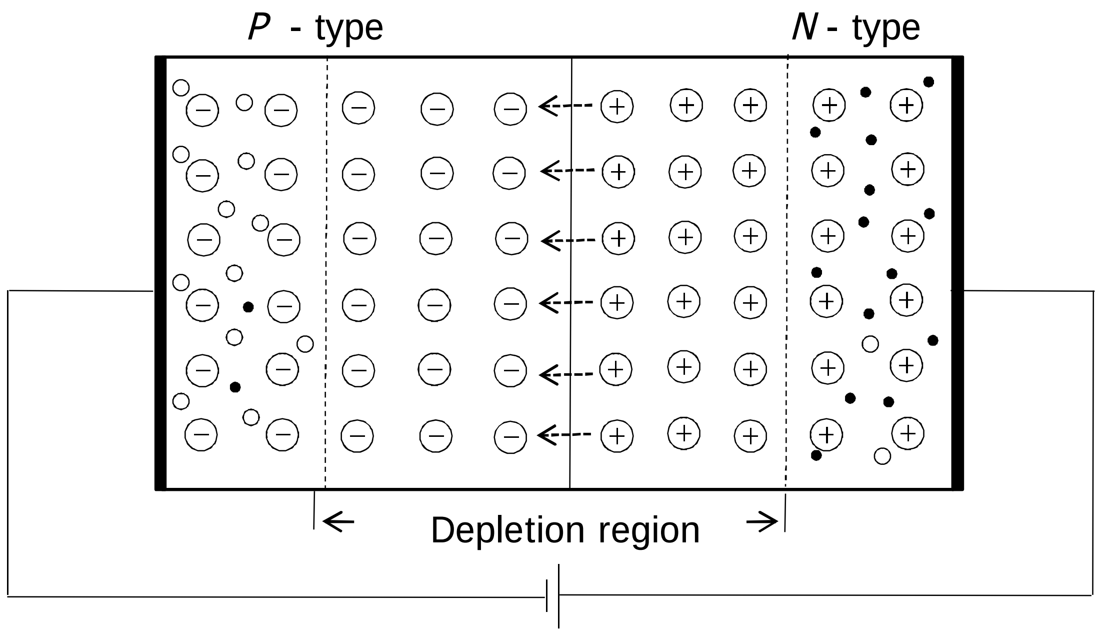




p-n junction forward biased

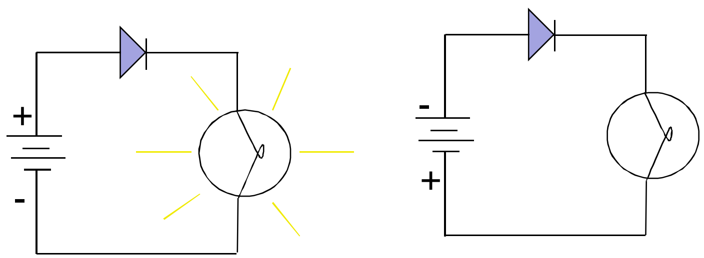


p-n junction reverse biased



Introduction

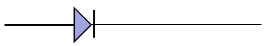
Diode operation



Current permitted
Diode is forward-biased

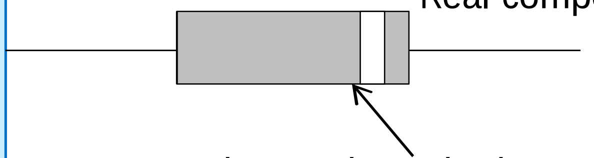
Current prohibited
Diode is reverse-biased

Anode Cathode

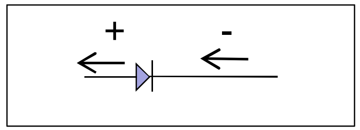


Schematic symbol

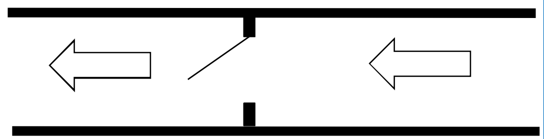
Real component appearance



Stripe marks cathode

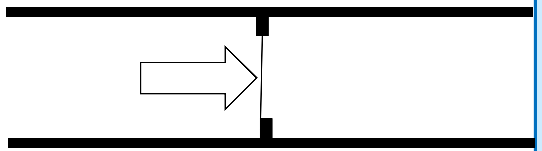


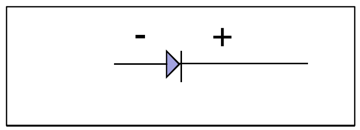
Flow permitted



Hydraulic check valve

Flow permitted





Contd.

$$I_D = I_S\left(e^{\frac{qV}{NkT}} - 1\right)$$

I_D ------- diode current

I_S ------- saturation current

e ------- Euler's Constant(2.71828....)

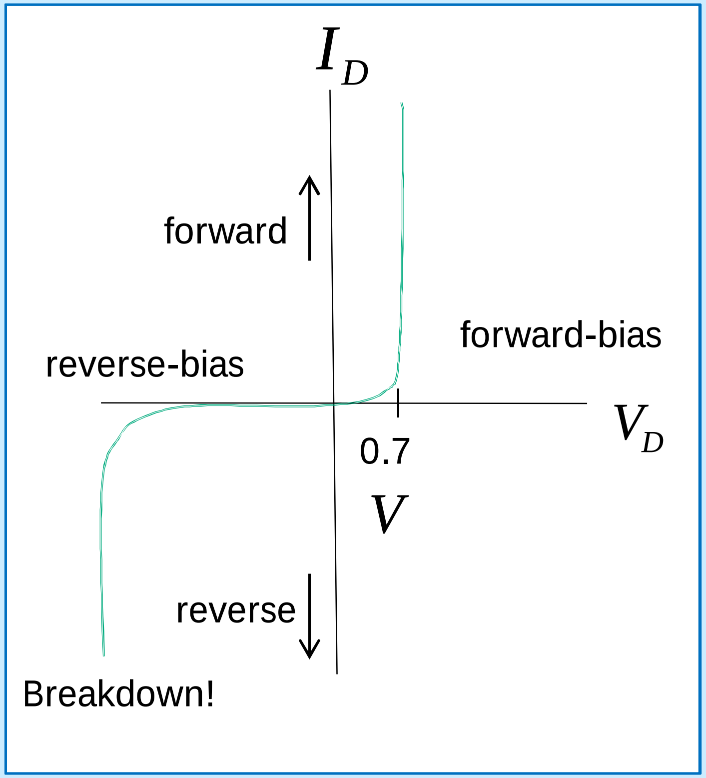
q ------- Charge of electron(1.6 $\bullet 10^{-19}$ As)

V ------- Voltage across the diode

N -------"Non-ideality" coefficient(typ.between 1 and 2)

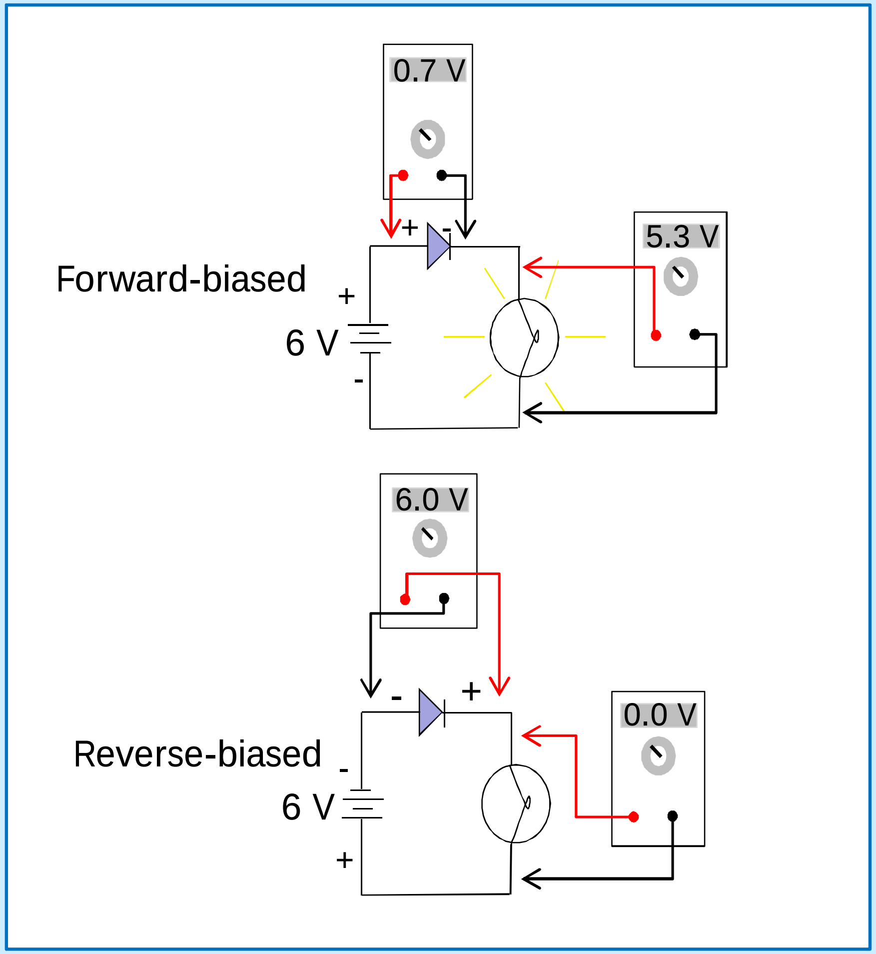
k ------- Boltzmann's constant (1.38) $\bullet 10^{-23}$)

T ------- Junction temperature in kelvin



$$I_D = I_S\left(e^{V_D/0.026} - 1\right)$$

Example

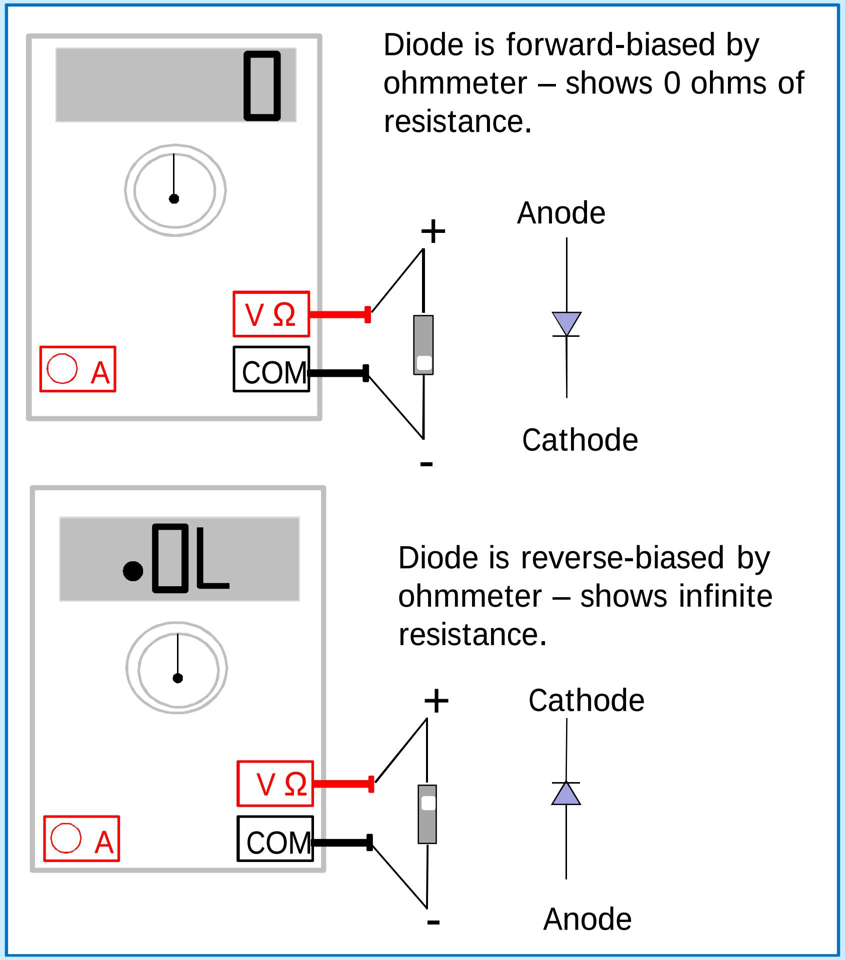


Summary

- A *diode* is an electrical component acting as a one-way valve for current.
- When voltage is applied across a diode in such a way that the diode allows current, the diode is said to be *forward-biased*.
- When voltage is applied across a diode in such a way that the diode prohibits current, the diode is said to be *reverse-biased*.
- The voltage dropped across a conducting, forward-biased diode is called the *forward voltage*. Forward voltage for a diode varies only slightly for changes in forward current and temperature, and is fixed principally by the chemical composition of the P-N junction.
- Silicon diodes have a forward voltage of approximately 0.7 volts.
- Germanium diodes have a forward voltage of approximately 0.3 volts.
- The maximum reverse-bias voltage that a diode can withstand without "breaking down" is called the *Peak Inverse Voltage*, or *PIV* rating.

Meter check of a diode

- Connected one way across the diode, the meter should show a very low resistance.
- Connected the other way across the diode, it should show a very high resistance ("OL" on some digital meter models)



Problem

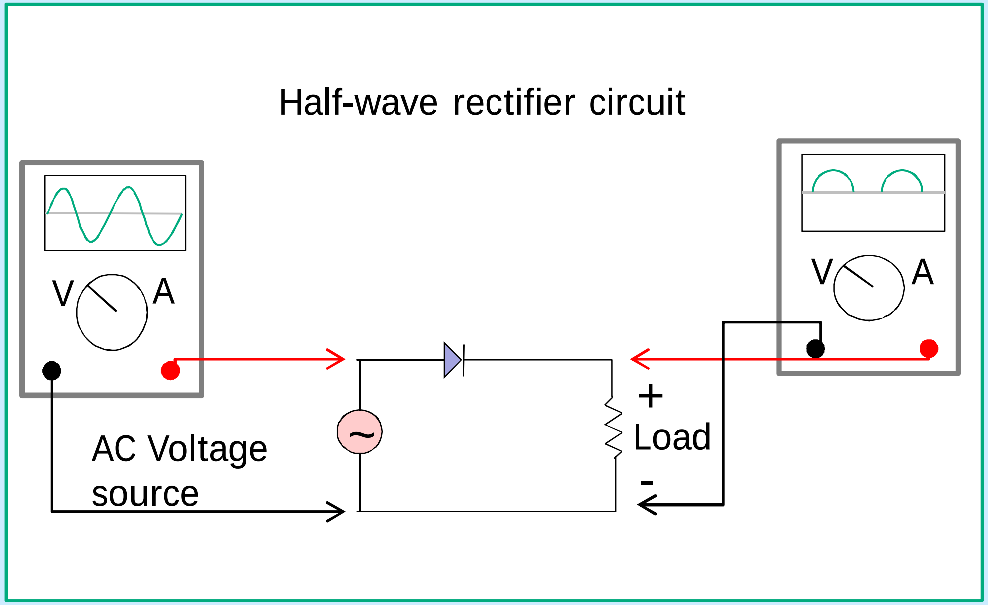
- Find out Application of Diodes

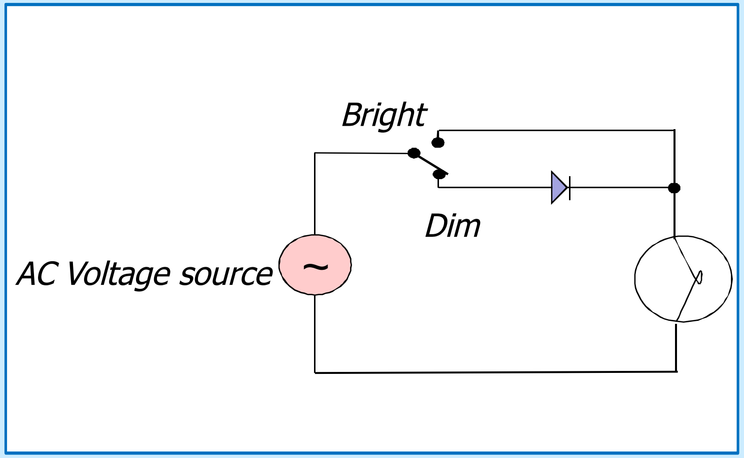
Rectifier Circuits

Rectification is the conversion of alternating current (AC) to direct current (DC).

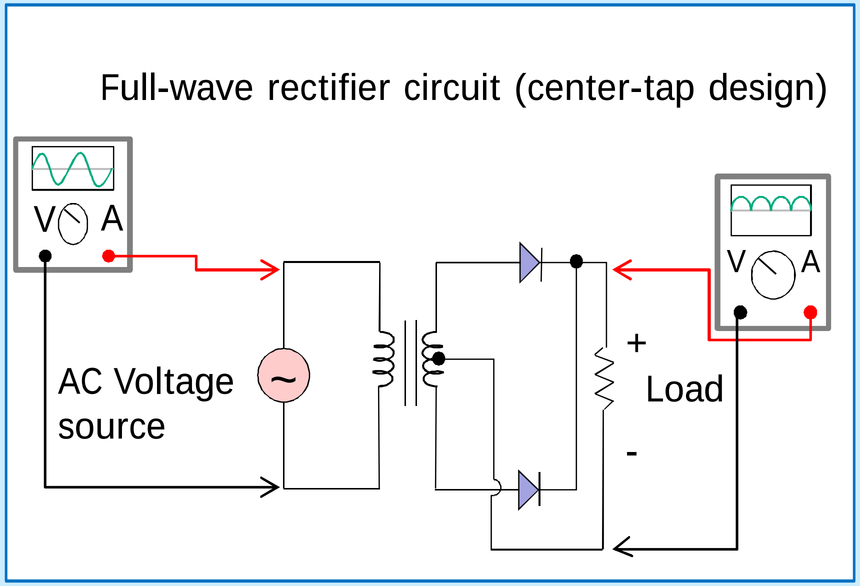
- A *half-wave* rectifier is a circuit that allows only one half-cycle of the AC voltage waveform to be applied to the load, resulting in one non-alternating polarity across it. The resulting DC delivered to the load "pulsates" significantly.
- A *full-wave* rectifier is a circuit that converts both half-cycles of the AC voltage waveform to an unbroken series of voltage pulses of the same polarity. The resulting DC delivered to the load doesn't "pulsate" as much.

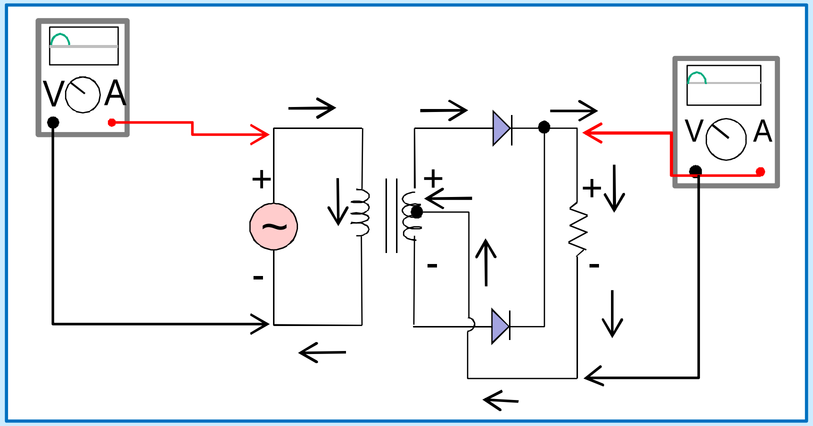
Half-wave Rectifier

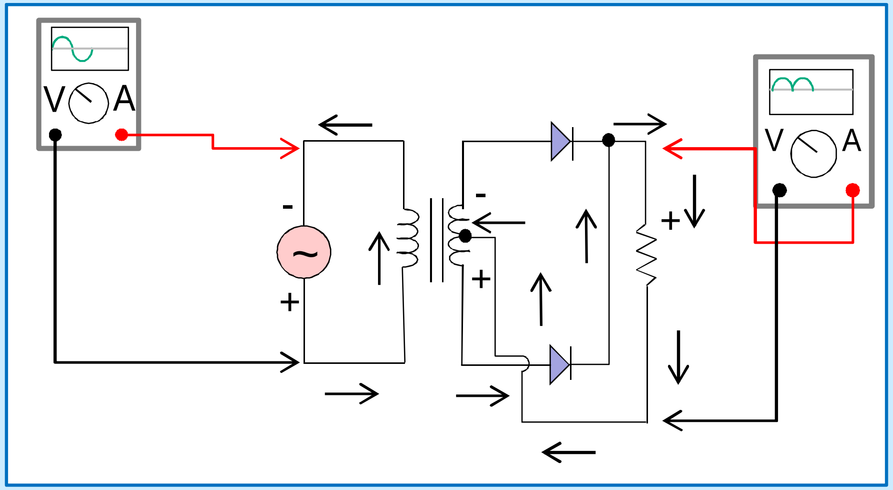




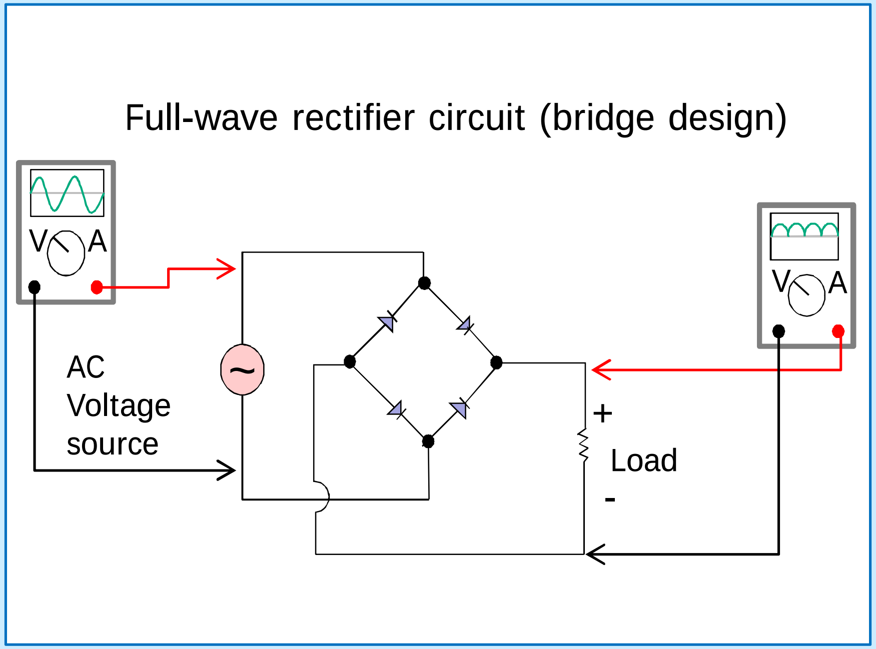
Full-wave Rectifier

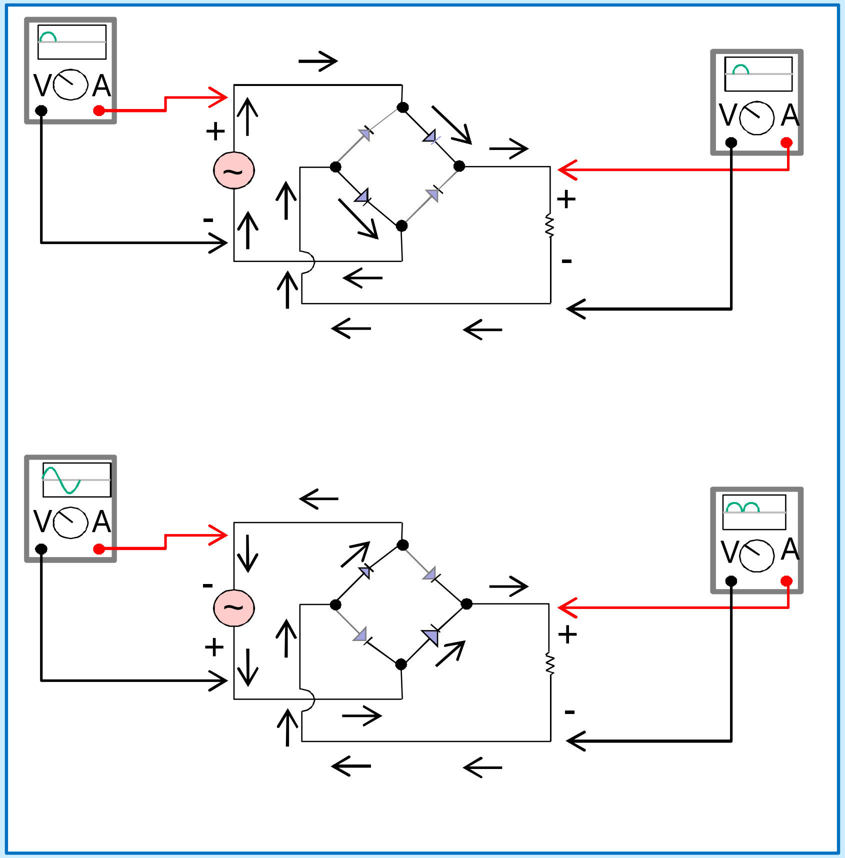






Full wave bridge rectifier





Diode ratings

In addition to forward voltage drop (Vf) and peak inverse voltage (PIV), there are many other ratings of diodes

- **Maximum DC reverse voltage = V_R or V_{DC}** The maximum amount of voltage the diode can withstand in reverse-bias mode on a continual basis. Ideally, this figure would be infinite.

- **Maximum reverse current = I_R** the amount of current through the diode in *reverse-bias* operation, with the maximum rated inverse voltage applied (V_{DC}). Sometimes referred to as *leakage current*. Ideally, this figure would be zero, as a perfect diode would block all current when reverse-biased. In reality, it is very small compared to the maximum forward current.

Contd.

- **Maximum (average) forward current = $I_{F(AV)}$** The maximum average amount of current the diode is able to conduct in forward bias mode. ***This is fundamentally a thermal limitation***: how much heat can the PN junction handle, given that dissipation power is equal to current (I) multiplied by voltage (V or E) and forward voltage is dependent upon both current and junction temperature. Ideally, this figure would be infinite.

- **Maximum (peak or surge) forward current = I_{FSM} or $i_{f(surge)}$** The maximum peak amount of current the diode is able to conduct in forward bias mode. Again, ***this rating is limited by the diode junction's thermal capacity***, and is usually much higher than the average current rating due to thermal inertia (the fact that it takes a finite amount of time for the diode to reach maximum temperature for a given current). Ideally, this figure would be infinite.

Contd.

- **Maximum total dissipation = P_D** The amount of power (in watts) allowable for the diode to dissipate, given the dissipation (P=IE) of diode current multiplied by diode voltage drop, and also the dissipation ($P=I^2R$) of diode current squared multiplied by bulk resistance. ***Fundamentally limited by the diode's thermal capacity*** (ability to tolerate high temperatures).

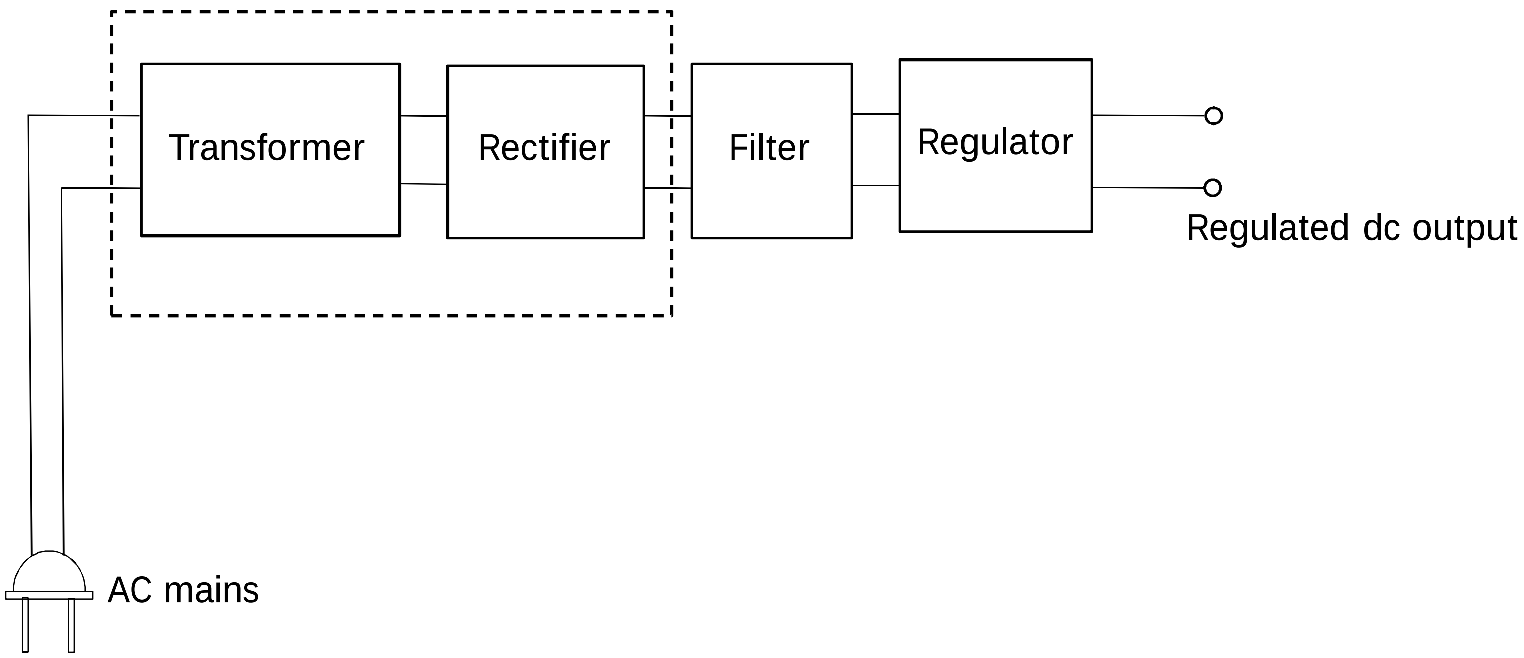
- **Operating junction temperature** = T_J The maximum allowable temperature for the diode's PN junction, usually given in degrees Celsius (^oC). Heat is the "Achilles' heel" of semiconductor devices: they *must* be kept cool to function properly and give long service life.

Contd.

- **Typical junction capacitance = C_J** the typical amount of capacitance intrinsic to the junction, due to the depletion region acting as a dielectric separating the anode and cathode connections. This is usually a very small figure, measured in the range of picofarads (pF).

- **Reverse recovery time = t_{rr}** the amount of time it takes for a diode to "turn off" when the voltage across it alternates from forward-bias to reverse-bias polarity. Ideally, this figure would be zero

Power Supply

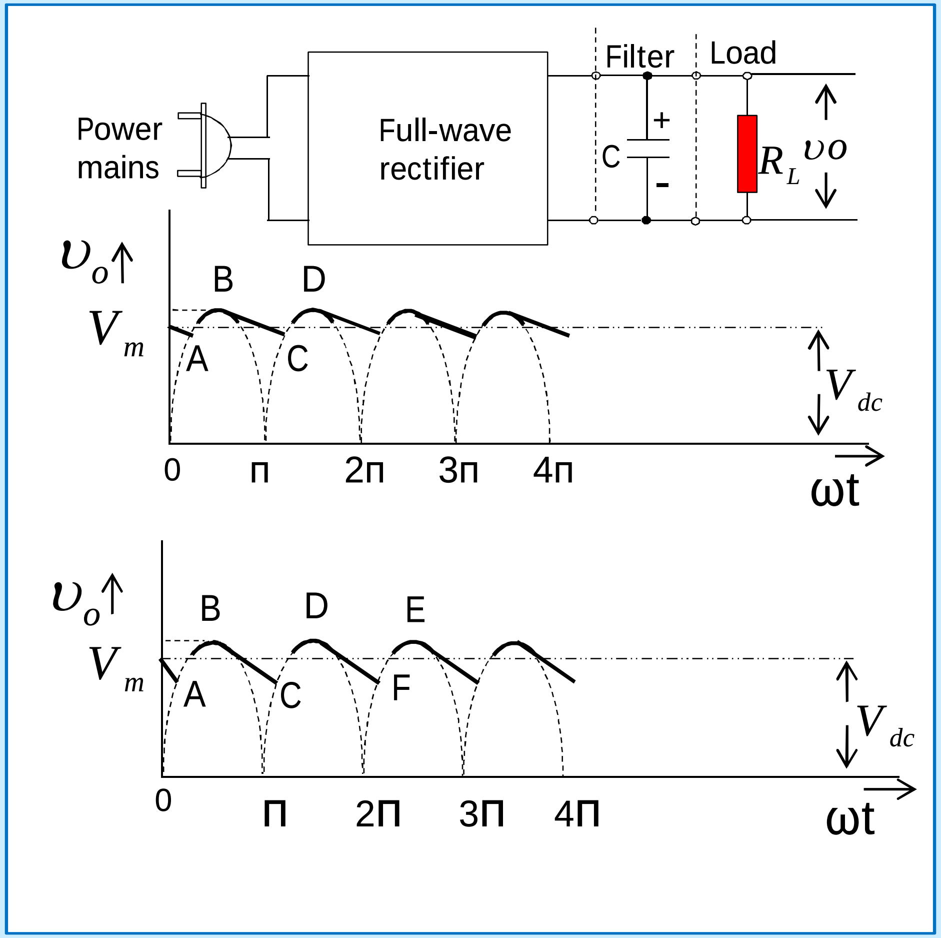


Need of Filter

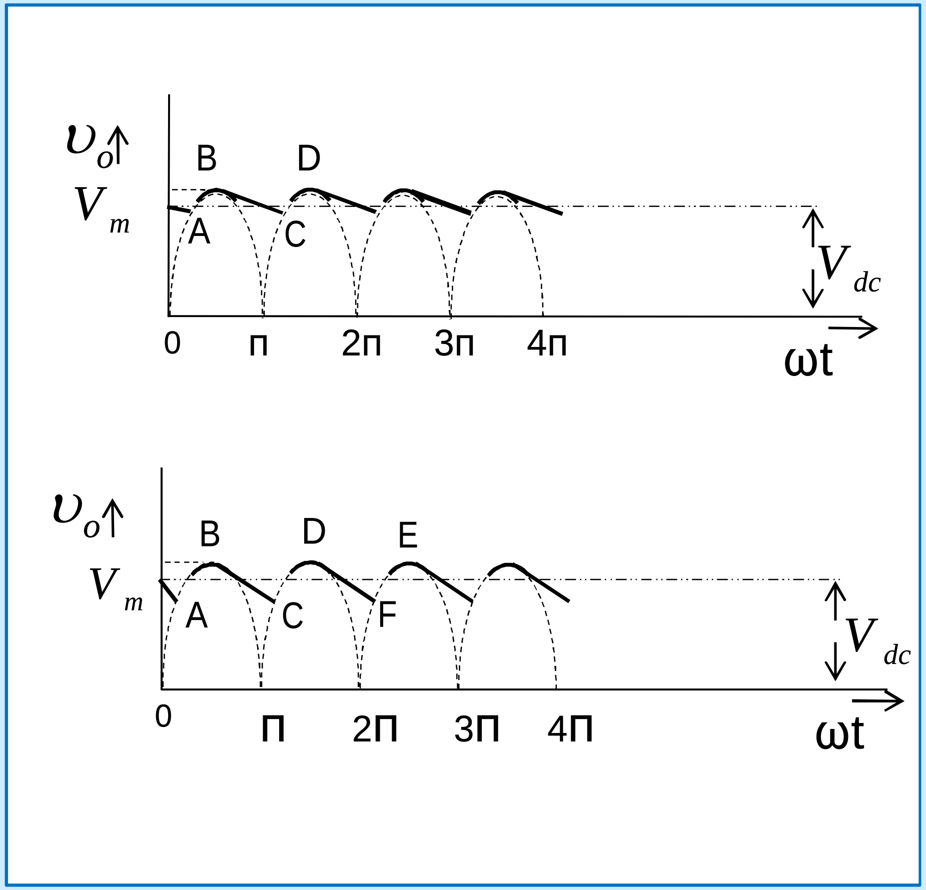
- Full-wave rectifier output is not smooth, it has lot of ripples
- In order to minimize these ripples, a filter is required to smooth the out of full wave rectifier.

Shunt Capacitor Filter

- Shunt capacitor is simplest and cheapest type filter
- Connect a large value of capacitor across load
- Block DC, allow AC to follow
- Rate of discharge depend on $R_L C$
- Large C give less ripples
- Upper limit of C depends on current handling rating of diodes



Conduction angle of diode



Ripple voltage

$$V = \frac{Q}{C}$$

$$V_1 = \frac{Q_1}{C}$$

$$V_2 = \frac{Q_2}{C}$$

$$V_1 - V_2 = \frac{Q_1 - Q_2}{C}$$

$$\frac{V_1 - V_2}{T_1 - T_2} = \frac{Q_1 - Q_2}{C(T_1 - T_2)}$$

$$\frac{V_1 - V_2}{T} = \frac{Q_1 - Q_2}{CT}$$

$$\frac{V_1 - V_2}{T} = \frac{I}{C}$$

$$V_{rip} = \frac{I}{fC}$$

$V_{rip} =$ peak-to-peak ripple voltage

$I =$ dc load current

$f =$ ripple frequency

$C =$ capacitance

$$V_{dc} = V_{2(peak)} - \frac{V_{rip}}{2}$$

Problem

Load current = 10 mA

Capacitance= 470 μF

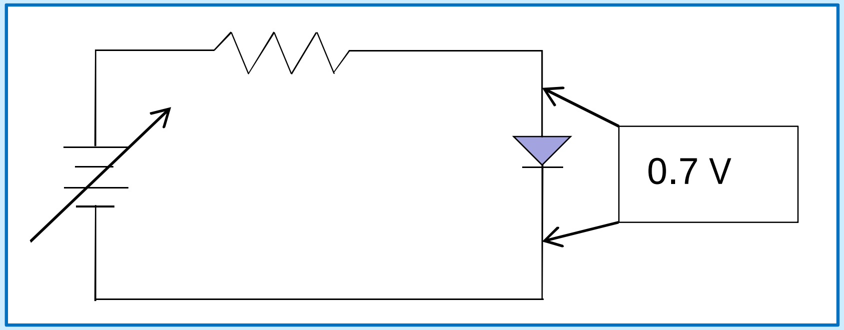
Line frequency = 50 Hz

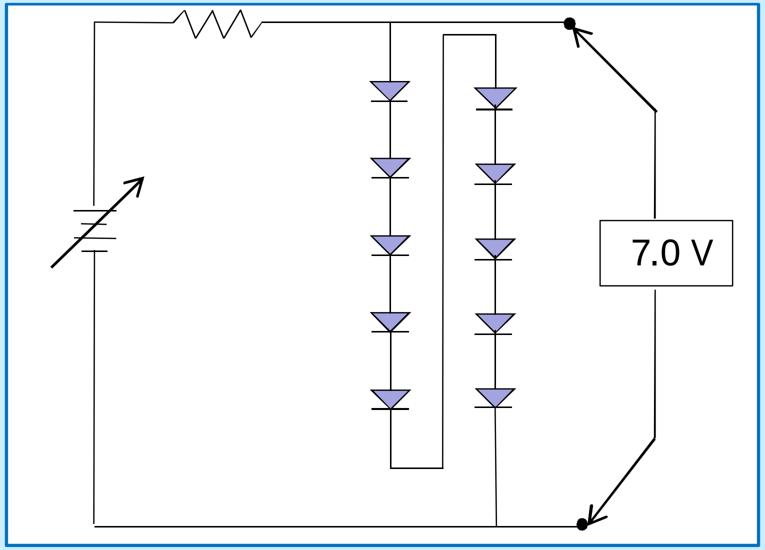
Find ripple voltage of full wave rectifier and half wave rectifier

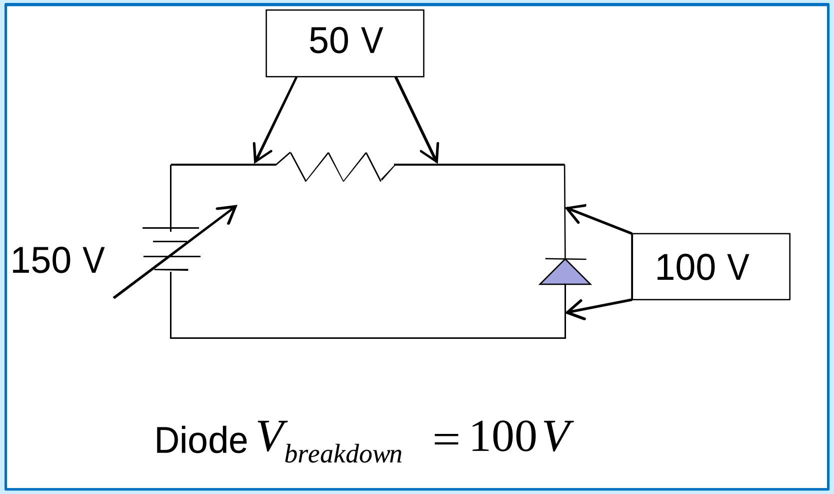
Need of Regulator

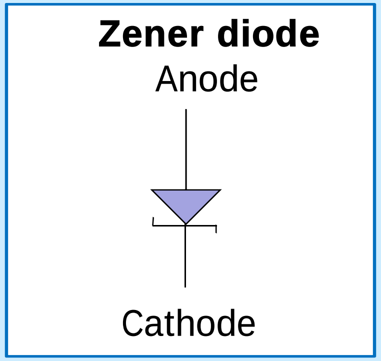
- Output of filter also have some ripples, to make it more smooth, regulator is required.
- Zener diode is one of the simplest type of regulator

Zener diodes









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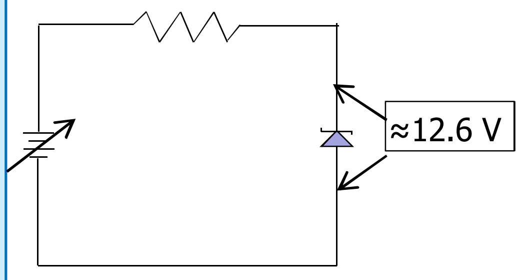
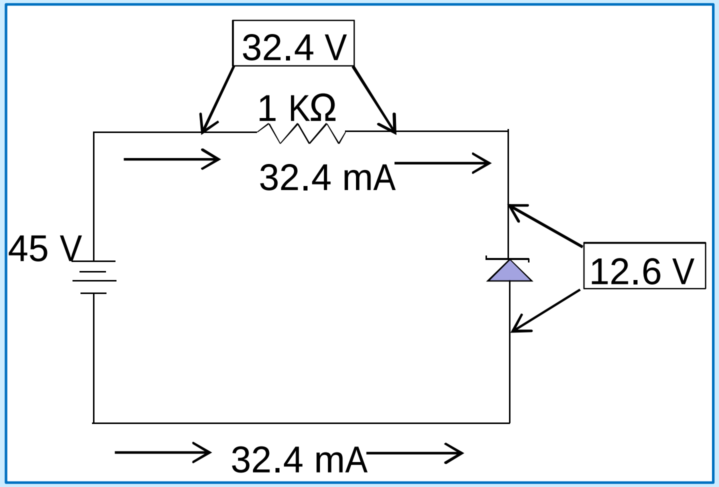


Diode $V_{zener} = 12.6V$

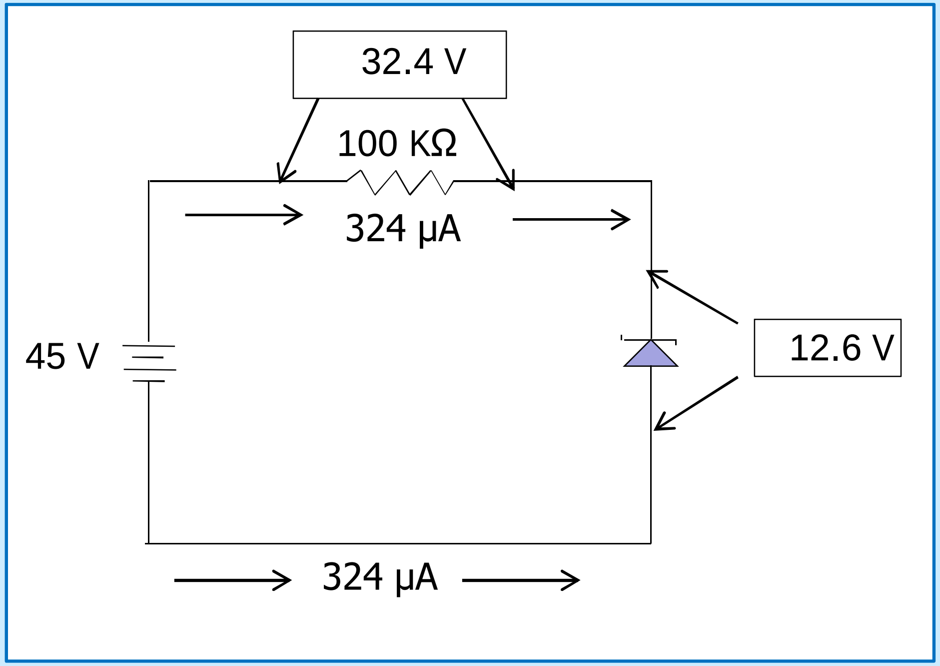


$$P_{resistor} = (32.4\text{mA})(32.4\text{V})$$
$$P_{resistor} = 1.0498\text{W}$$

$$P_{diode} = (32.4\text{mA})(12.6\text{V})$$
$$P_{diode} = 408.24\text{mW}$$

A zener diode with a power rating of 0.5 watt would be adequate, as would a resistor rated for 1.5 or 2 watts of dissipation.

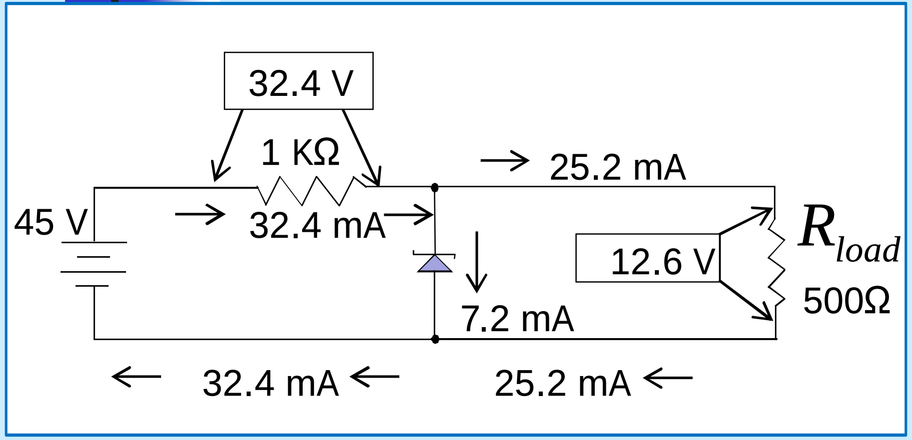
Contd.

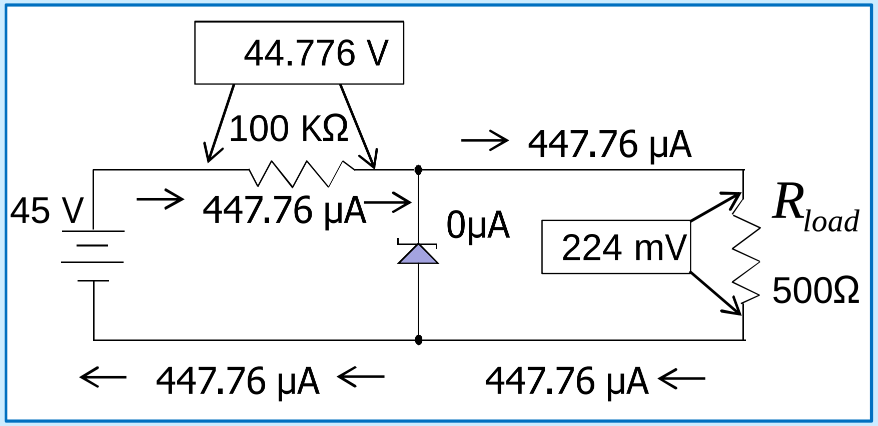


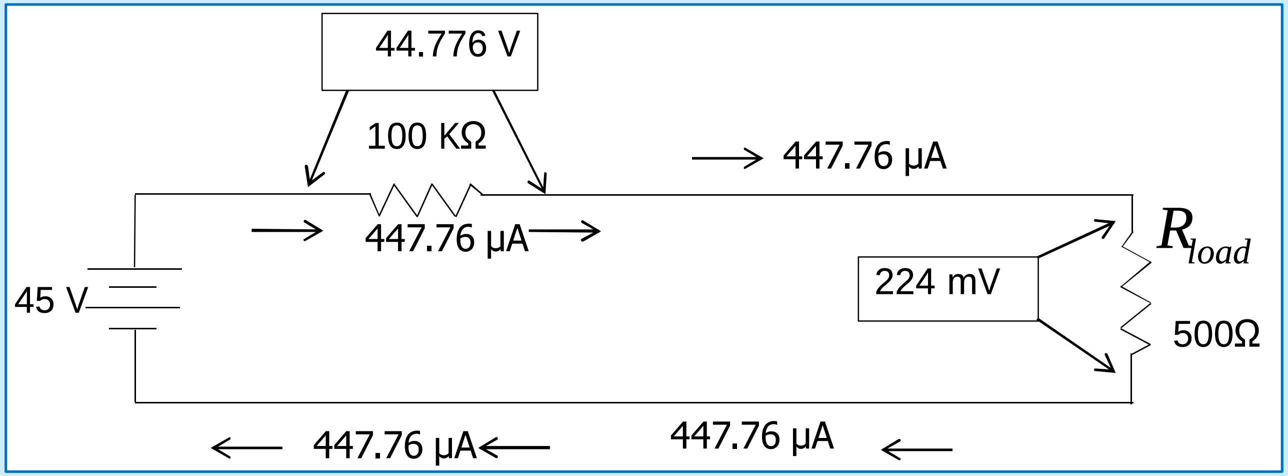
$$P_{resistor} = (324\mu A)(32.4V)$$
$$P_{resistor} = 10.498mW$$

$$P_{diode} = (324\mu A)(12.6V)$$
$$P_{diode} = 4.0824mW$$

Contd.


32.4 V
1 KΩ
25.2 mA
45 V
32.4 mA
12.6 V
R load
500Ω
7.2 mA
32.4 mA
25.2 mA


44.776 V
100 KΩ
447.76 μA
45 V
447.76 μA
0μA
224 mV
R load
500Ω
447.76 μA
447.76 μA


44.776 V
100 KΩ
447.76 μA
447.76 μA
45 V
224 mV
R load
500Ω
447.76 μA
447.76 μA

Schottky diodes

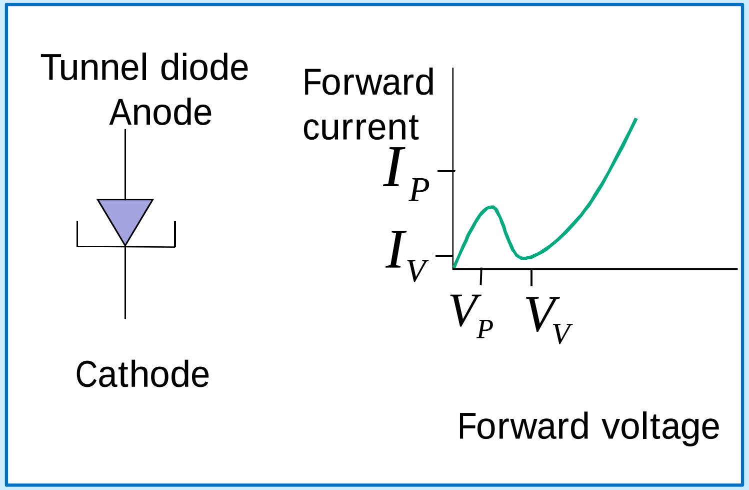
- *Schottky diodes* are constructed of a ***metal*-to-N junction** rather than a P-N semiconductor junction.
- Schottky diodes are characterized by fast switching times (low reverse-recovery time), low forward voltage drop (typically 0.25 to 0.4 volts for a metal-silicon junction), and low junction capacitance. This makes them ***well suited for high-frequency applications***.
- In terms of forward voltage drop (V_F), reverse-recovery time (t_{rr}), and junction capacitance (C_J), Schottky diodes are closer to ideal than the average "rectifying" diode. Unfortunately, though, ***Schottky diodes typically have lower forward current (*** I_F ***) and reverse voltage (*** V_{RRM} ***and*** V_{DC} ***)*** ratings than rectifying diodes and are thus unsuitable for applications involving substantial amounts of power.

Tunnel diodes

- *Tunnel diodes* ***exploit a strange quantum phenomenon*** called *resonant tunneling* to provide interesting forward-bias characteristics ***having peak current (I_P) Valley current (I_V).***

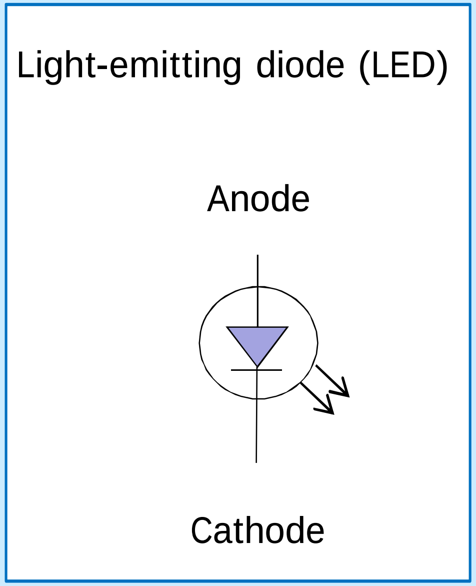
- Able to ***transition between peak and valley current levels very quickly***, "switching" between high and low states of conduction much faster than even Schottky diodes.

- Tunnel diode characteristics are also relatively ***unaffected by changes in temperature.***



Light-emitting diodes

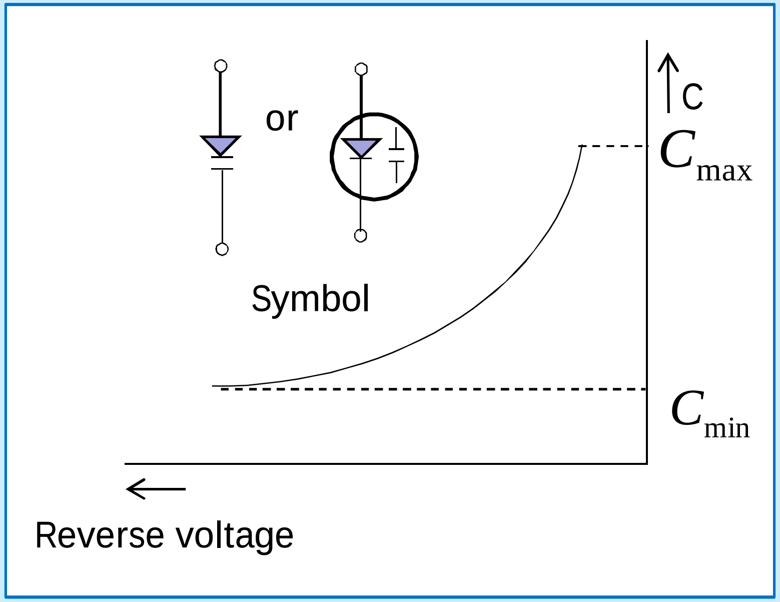
- Some semiconductor junctions, ***composed of special chemical combinations***, emit radiant energy within the spectrum of visible light as the electrons transition in energy levels.
- Simply put, these ***junctions glow when forward biased***. A diode intentionally designed to glow like a lamp is called a *light-emitting diode*, or *LED*.
- Diodes made from a combination of the elements ***gallium, arsenic, and phosphorus*** (called *gallium-arsenide-phosphide*) glow bright red, and are some of the most common LEDs manufactured



Varactor Diode

- It is ***operated reverse-biased*** so no current flows through it, but since the ***width of the depletion region varies with the applied bias voltage***, the capacitance of the diode can be made to vary.

- Varactors are commonly ***used in voltage-controlled oscillators***

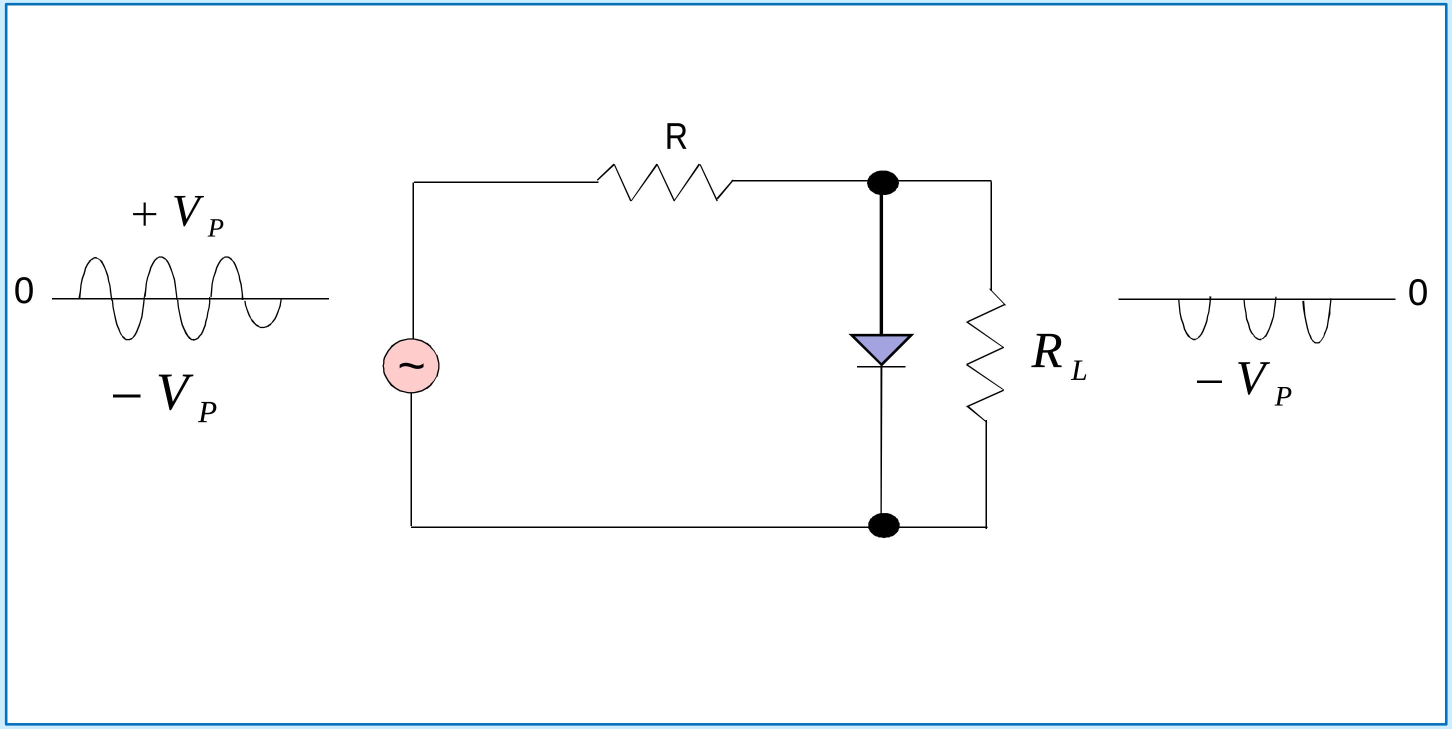


Limiter

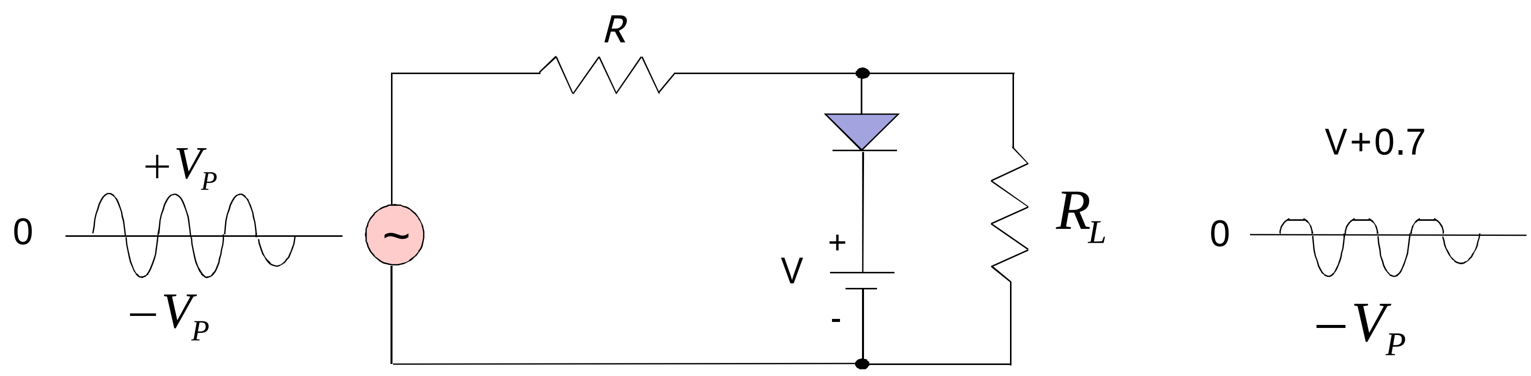
Limiter removes signal voltage above and below a specified level

- Useful for signal shaping, circuit protection etc.
- Use of small signal diode at high frequency.

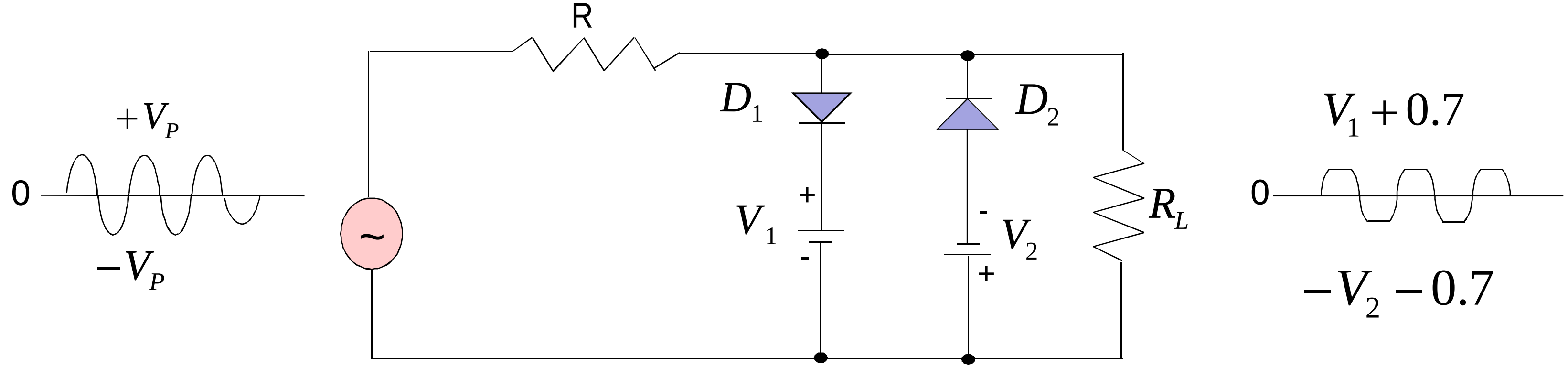
Positive Limiter



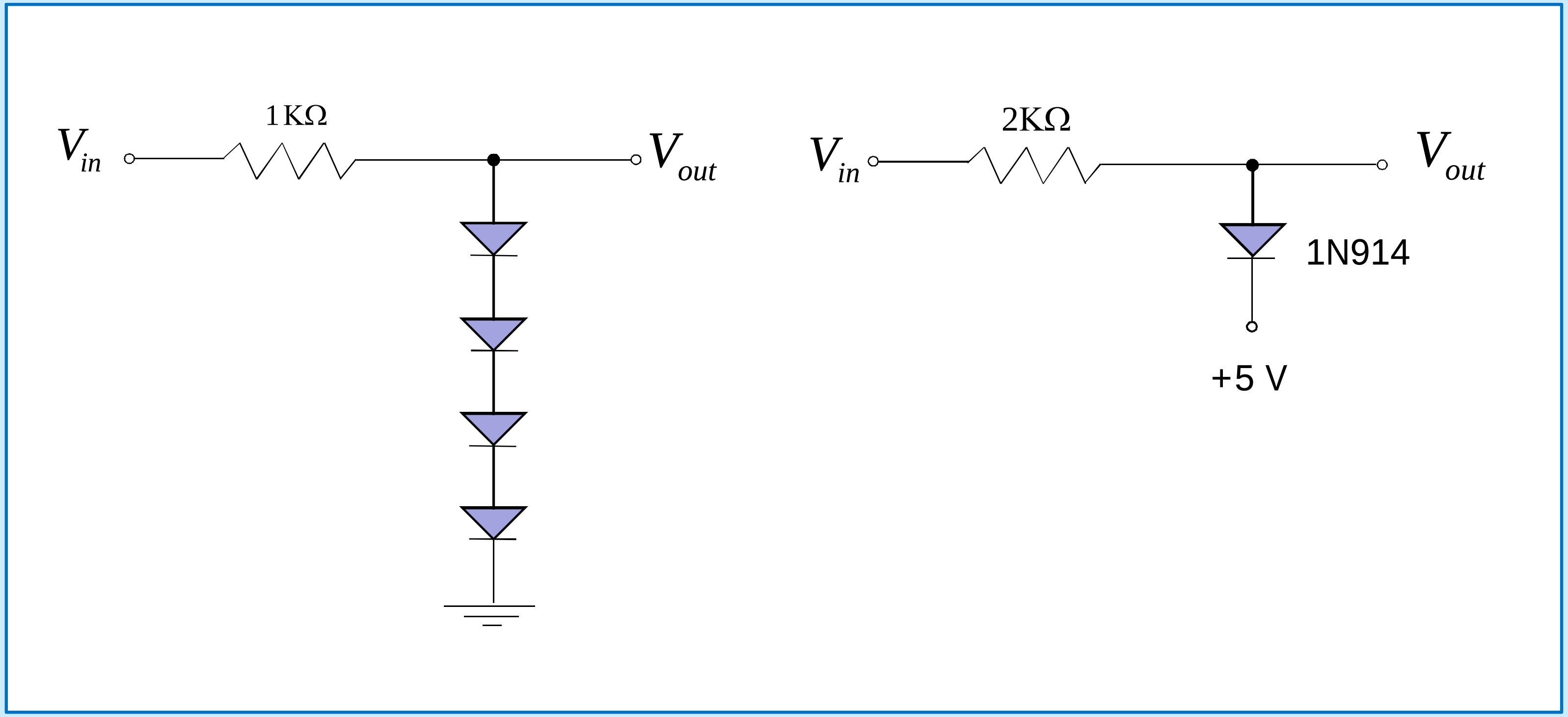
Biased limiter



Combination limiter



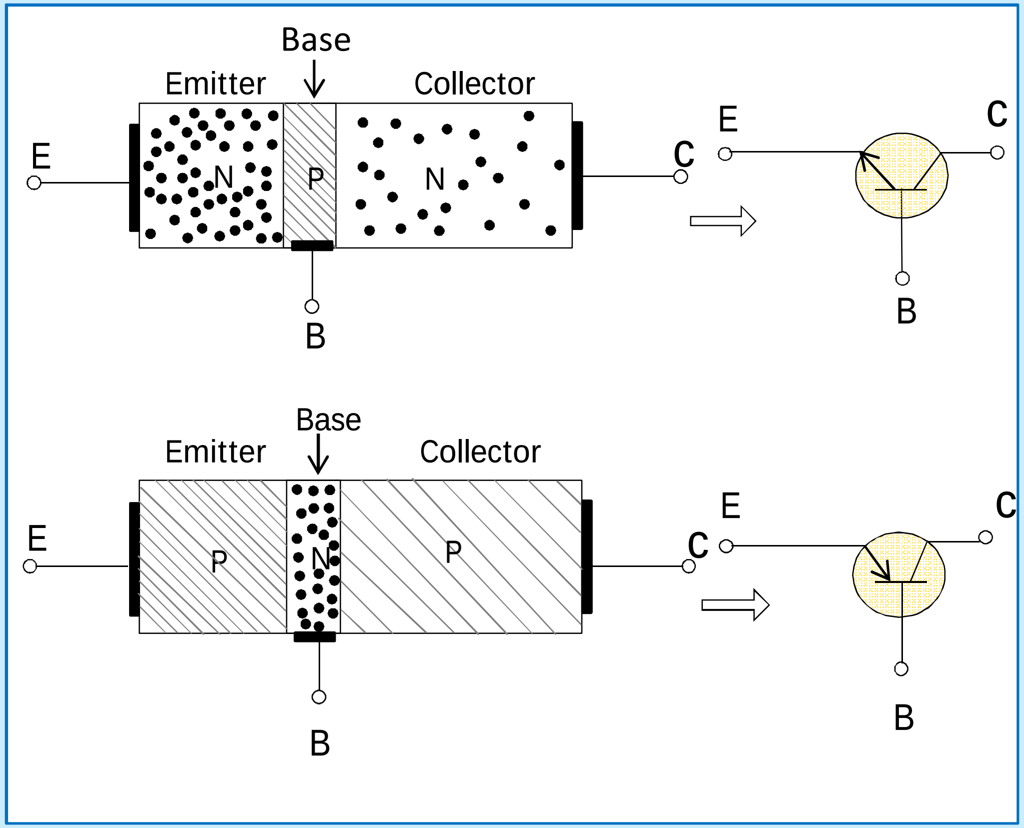
Circuit protection limiter



Transistors

Introduction

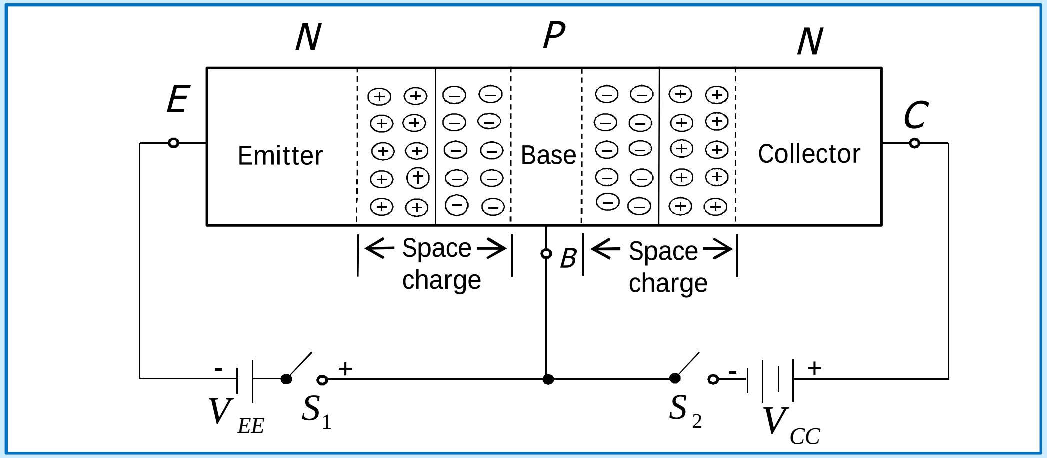
- The invention of the bipolar transistor in 1948 ushered in a revolution in electronics.
- Bipolar transistors consist of either a P-N-P or an N-P-N semiconductor "sandwich" structure.
- The three leads of a bipolar transistor are called the *Emitter*, *Base*, and *Collector*.
- Difference between PNP and NPN transistor is the proper biasing of junctions. Current directions and voltage polarities for each type of transistor are exactly opposite



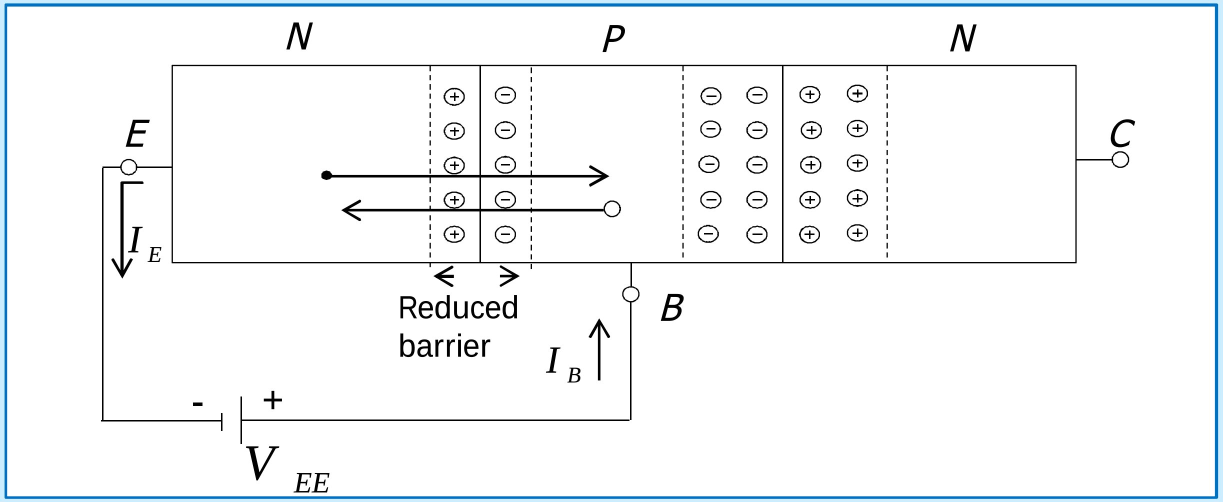
Transistor Mode of Operation

Condition	Emitter junction	Collector junction	Region of operation
FR	Forward-biased	Reverse-biased	Active
FF	Forward-biased	Forward-biased	Saturation
RR	Reverse-biased	Reverse-biased	Cutoff
RF	Reverse-biased	Forward-biased	Inverted

Biasing an NPN transistor for active operation

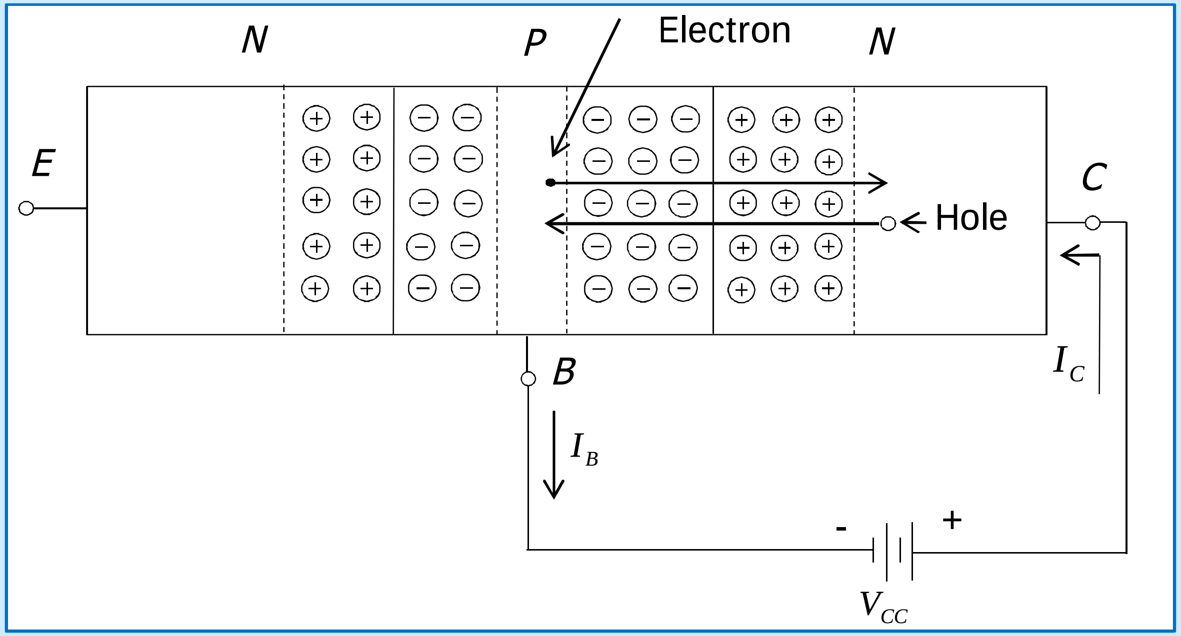


Only emitter junction forward biased



- Larger current flow
- ~ 99 % of total current carried by electrons (moving from emitter to base)
- Emitter current and base current very large (I_E=I_B), I_C=0

Only collector junction reverse biased



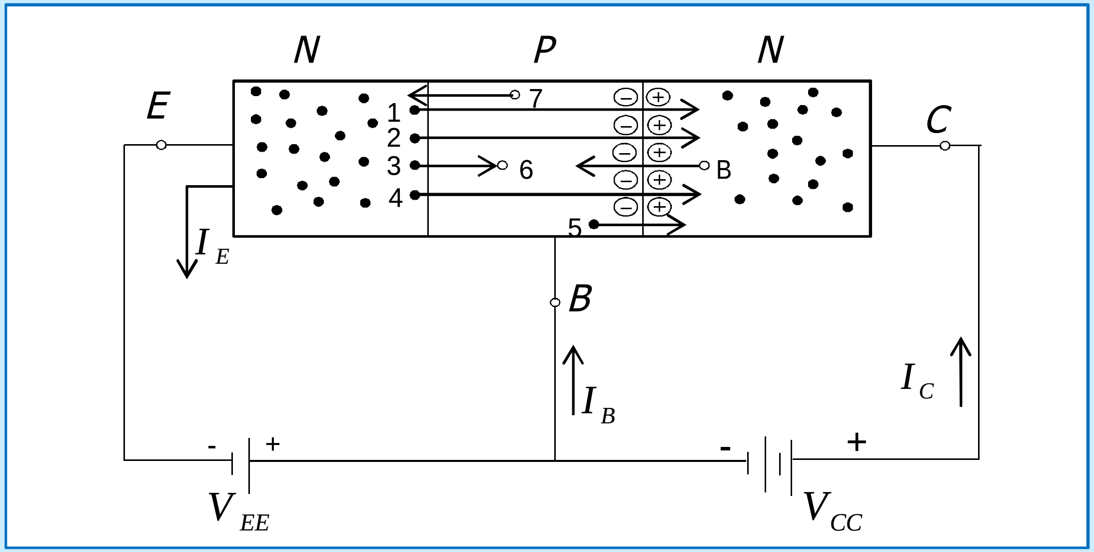
- Very small current flow (minority carrier current temperature dependent current) called collector leakage current I_{CBO}
- I_{CBO} signifies current between collector and base when third terminal (emitter) is open

Surprising action of transistor

If emitter junction forward biased and collector junction reverse biased

- Expectation
  - Both emitter and base current to be large and collector current very small
- Reality
  - Emitter current is large as expected, but base current turns out to be very small and collector current turns out to be large

Working of transistor



- Ratio of no. of electrons arriving at collector to no. of emitted electrons is know as base transportation factor (typically ~ 0.99)
- No. of electrons (like 3) and holes (like 7) crossing the E-B junction is much more than the no. of electrons (like 5) and holes (like 8) crossing the C-B junction. The difference of these two currents is base current.

Contd.

- Collector current is less than emitter current
  - A part or emitter current consists of holes that do not contribute to collector current
  - Not all the electrons injected into the base are successful in reaching collector.

  Ratio of collector current to emitter current is typically 0.99 denoted by α_{dc}
- Collector current made up of two parts
  - Fraction of emitter current which reaches the collector
  - Reverse leakage current I_{CO}

$$I_C = \alpha_{dc} I_E + I_{CO}$$

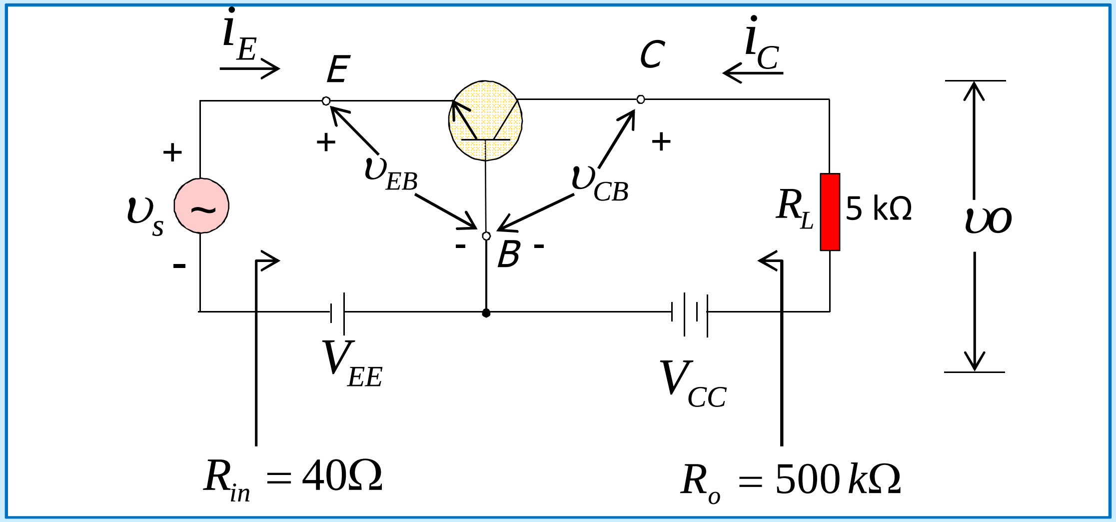
- Total current equation

$$I_E = I_C + I_B$$

Problem

- An NPN transistor has of α_{dc} 0.98 and a collector leakage current of 1 uA. Calculate the collector and base current, when emitter current is 1 mA.

Transistor amplifying action



$$I_e = \frac{20 \times 10^{-3}}{40} = 0.5mA$$

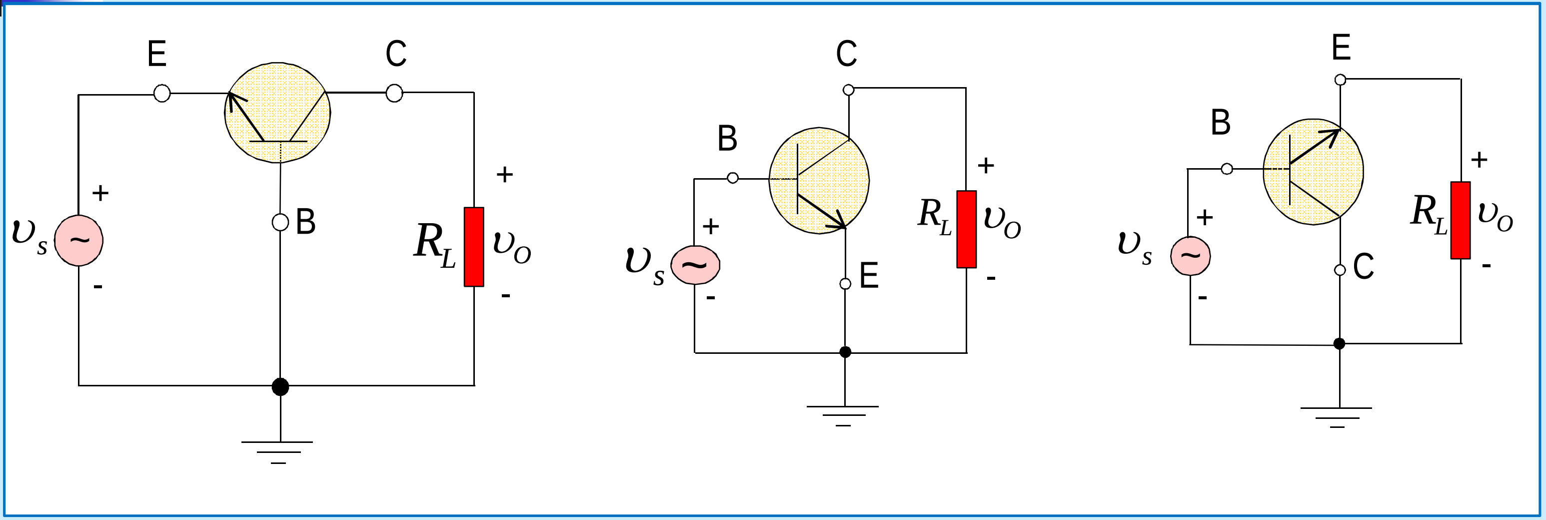
$$I_c \cong I_e = 0.5mA$$

$$V_O = I_c R_L$$
$$= (0.5 \times 10^{-3}) \times (5 \times 10^3) = 2.5V$$

Transfer + resistor = transistor

$$A_\upsilon = \frac{V_O}{V_S}$$
$$= \frac{2.5}{20 \times 10^{-3}} = 125$$

Different configurations of transistor



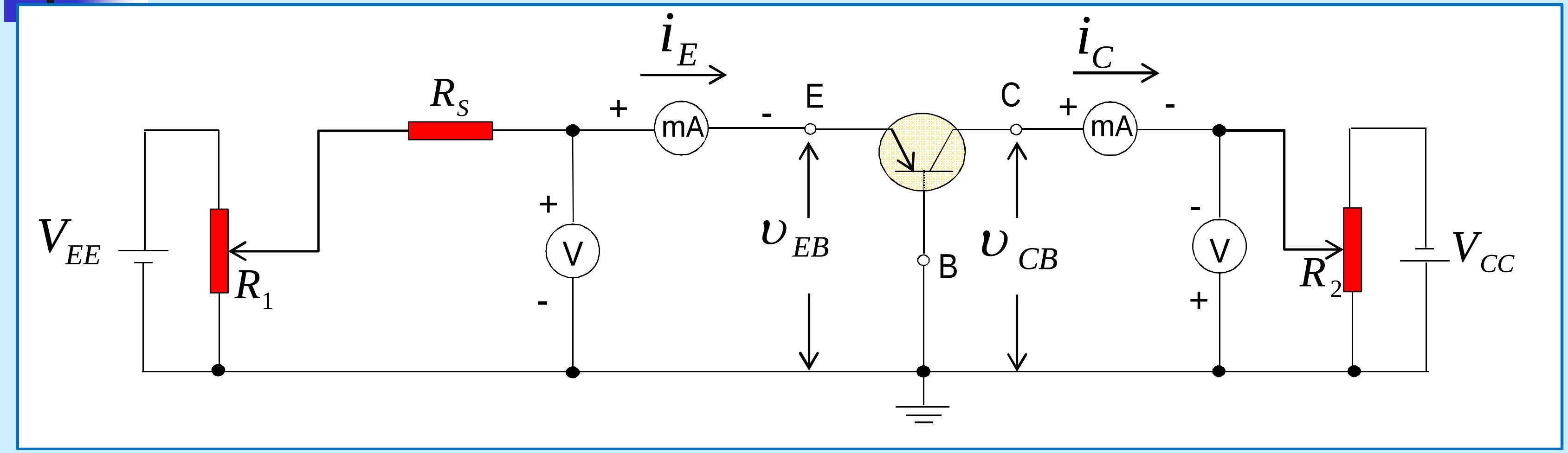
- Figure shows three configuration from ac point of view.
- In all configurations, emitter-base junction is always forward-biased and collector base junction is always reverse-biased.

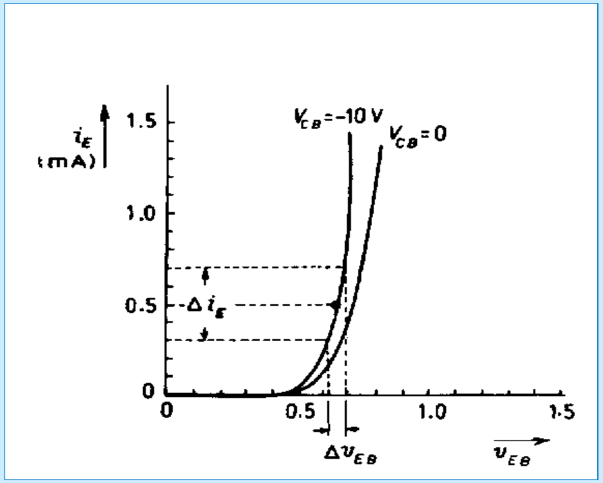
Transistor characteristics

Static characteristic curves to relate current and voltage in a transistor.

- Input characteristic
- Output characteristic

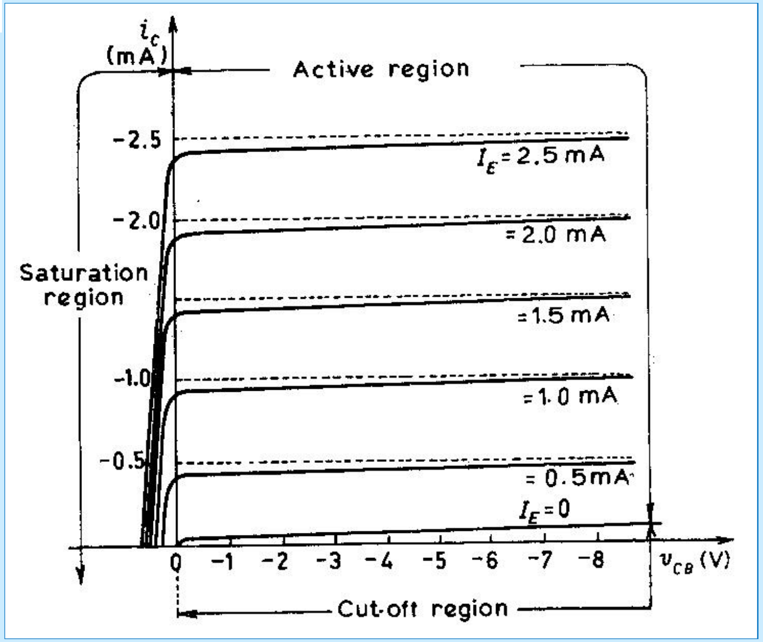
Common-Base Input characteristics





$$r_i = \left.\frac{\Delta \upsilon_{EB}}{\Delta i_E}\right|_{V_{CB} = Const.}$$

Common-Base output characteristics



$$r_o = \frac{\Delta \upsilon_{CB}}{\Delta i_C}\Bigg|_{I_E = Const.}$$

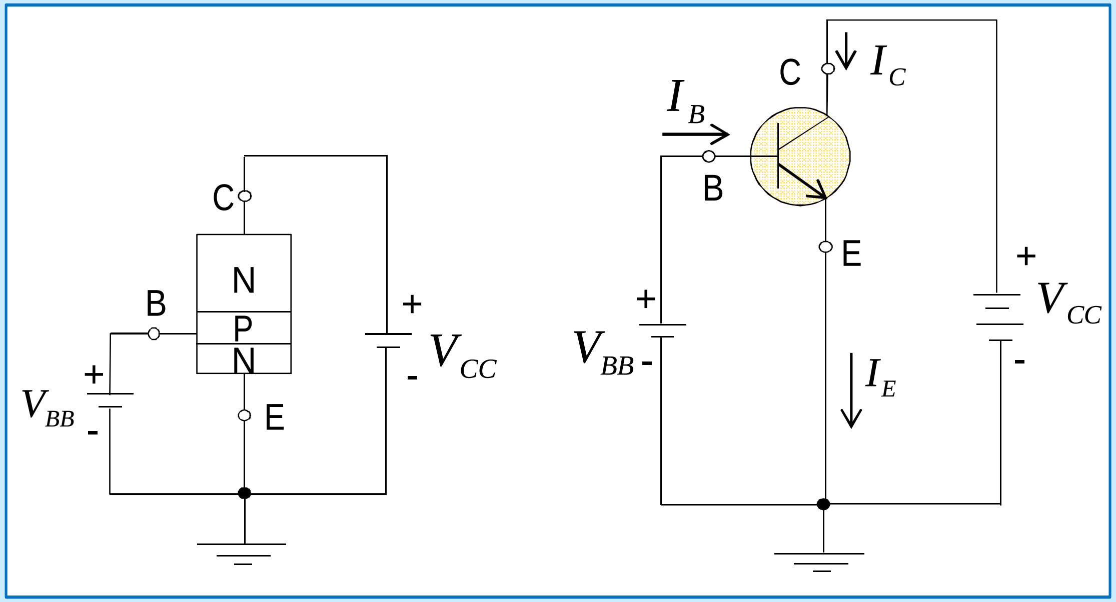
$$h_{fb} \, or \, \alpha = \frac{\Delta i_C}{\Delta i_E}\Bigg|_{V_{CB} = Const.}$$

- High output resistance – can be good current source
- Saturation region - collector current not remain same with change in emitter current
- Cut-off region- collector current is not zero even emitter current is zero due to leakage current I_{CB0} OR I_{CO}

Summary of C-B characteristics

- Current gain slightly less then unity (~0.98)
- Dynamic input resistance very low (~ 20 ohm)
- Dynamic output resistance very high (~ 1 M ohm)
- Leakage current very low (~ 0.02 uA for Si transistor)

C-E Configuration



$$I_C = \alpha_{dc}(I_C + I_B) + I_{CBO}$$

$$(1-\alpha_{dc})I_C = \alpha_{dc} I_B + I_{CBO}$$

$$I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B + \frac{1}{1-\alpha_{dc}} I_{CBO}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha_{dc}}$$

Mostly work in active region

$$I_C = \beta_{dc} I_B + I_{CEO}$$

Contd.

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$\beta_{dc} - \beta_{dc}\alpha_{dc} = \alpha_{dc}$$

$$\beta_{dc} = \alpha_{dc}(1+\beta_{dc})$$

$$\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc}+1}$$

$$I_E = I_C + I_B$$

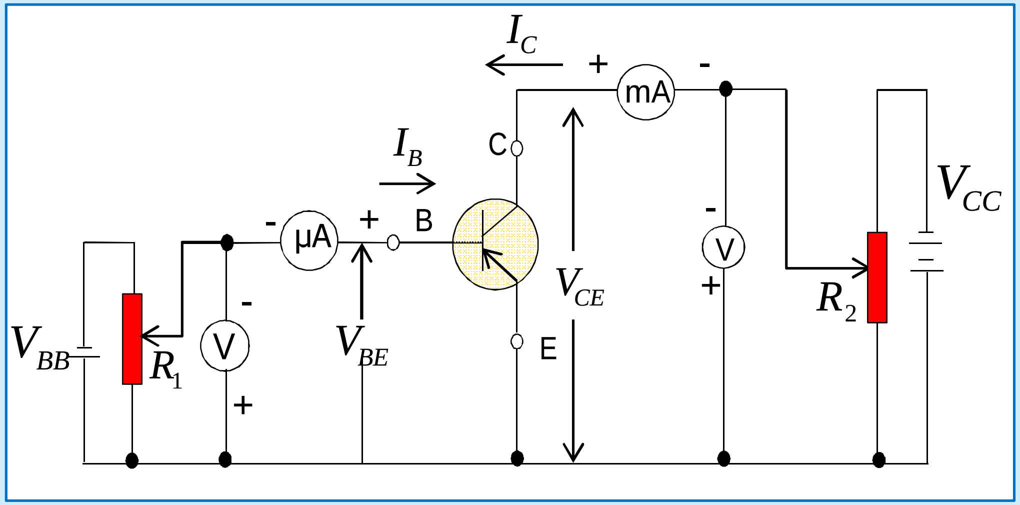
$$\Delta i_E = \Delta i_C + \Delta i_B$$

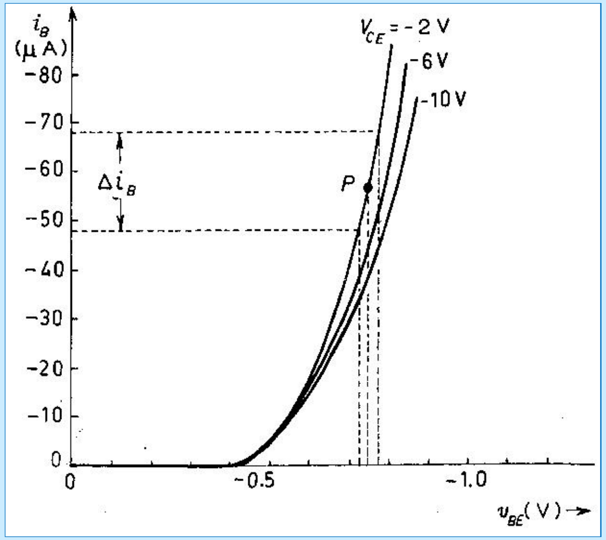
$$\frac{\Delta i_E}{\Delta i_C} = 1 + \frac{\Delta i_B}{\Delta i_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

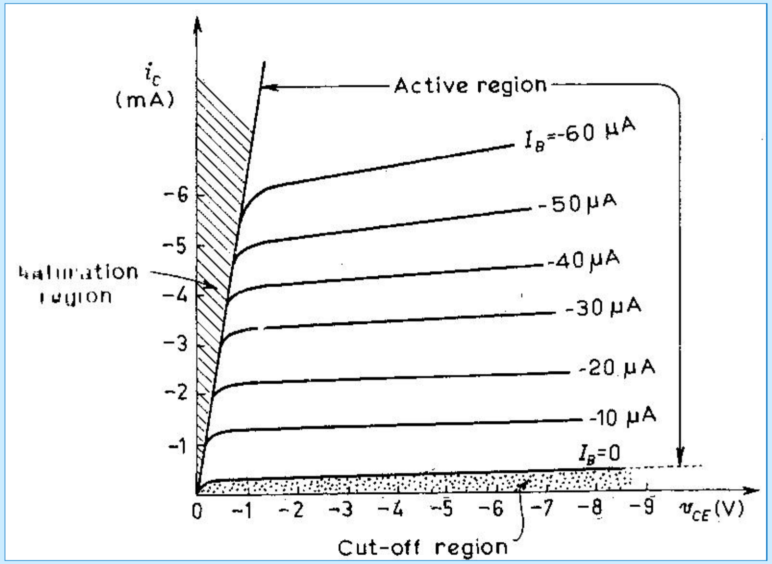
C-E input characteristics





$$r_i = \frac{\Delta \upsilon_{BE}}{\Delta i_B}\Bigg|_{V_{CE} = Const.}$$

C-E output characteristics



- Current gain increase with Vce
- Small base current produce large change in collector current
- Large leakage current I_{CEO}

Comparison between CB and CE

Parameters	Common – base Configuration	Common – emitter Configuration
1. Input dynamic resistance	Very low (20 Ω)	Low (1 kΩ)
2. Output dynamic resistance	Very high (1 MΩ)	High (10 kΩ)
3. Current gain	Less than unity (0.98)	High (100)
4. Leakage current	Very small (5 μA for Ge, 1 μA for Si)	Very large (500 μA for Ge, 20 μA for Si)

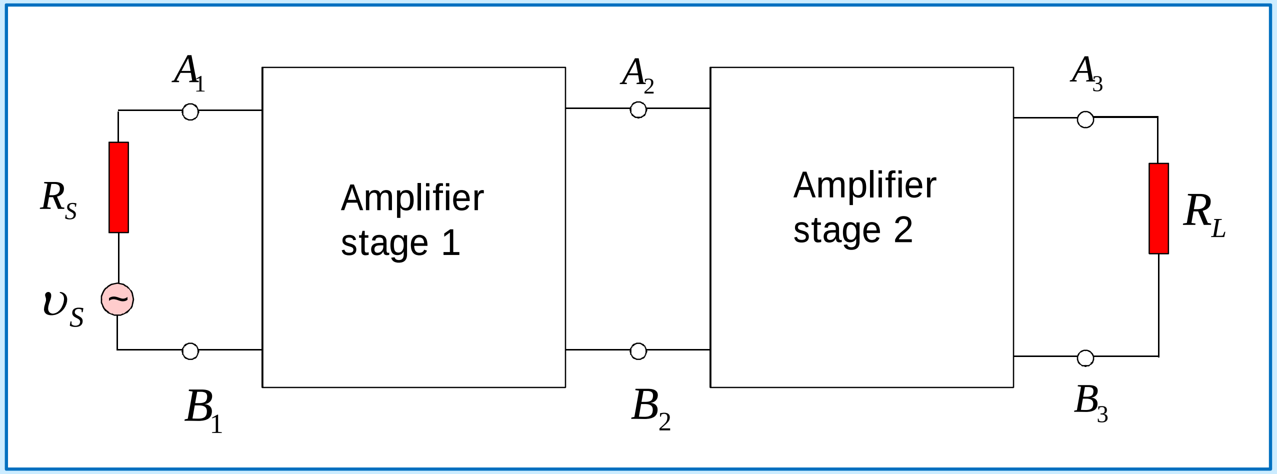
Leakage current lead to Thermal Runway

Problems

- When emitter current of transistor changed by 1mA, its collector current changed by 0.995 mA. Calculate
  - CB current gain
  - CE current gain

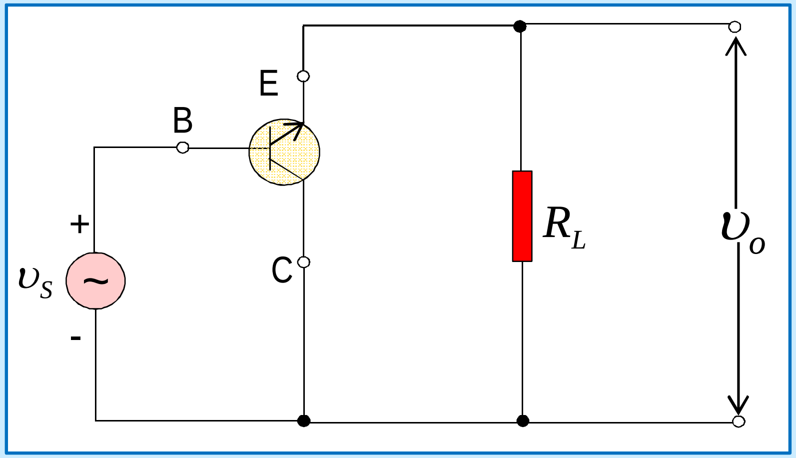
- The DC current gain of a transistor in CE configuration is 100. Find DC current gain in CB configuration.

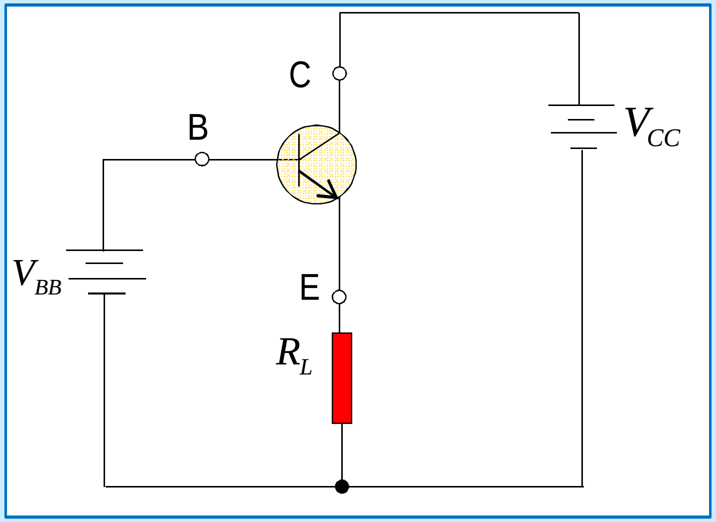
Why CE configuration widely used



- A good amplifier stage is one which has high input resistance and low output resistance
- Current gain is more in CE configuration

Common-collector configuration





Emitter current as a function of base current

$$I_E = I_B + I_C$$

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

Contd.

$$I_E = I_B + \alpha_{dc} I_E + I_{CBO}$$

$$(1-\alpha_{dc}) I_E = I_B + I_{CBO}$$

$$I_E = \frac{1}{1-\alpha_{dc}} I_B + \frac{1}{1-\alpha_{dc}} I_{CBO}$$

$$\frac{1}{1-\alpha_{dc}} = \beta_{dc} + 1$$

$$I_E = (\beta_{dc}+1) I_B + (\beta_{dc}+1) I_{CBO}$$

$$I_E = (\beta_{dc}+1) I_B$$

$$\frac{I_E}{I_B} = (\beta_{dc}+1)$$

CC characteristics

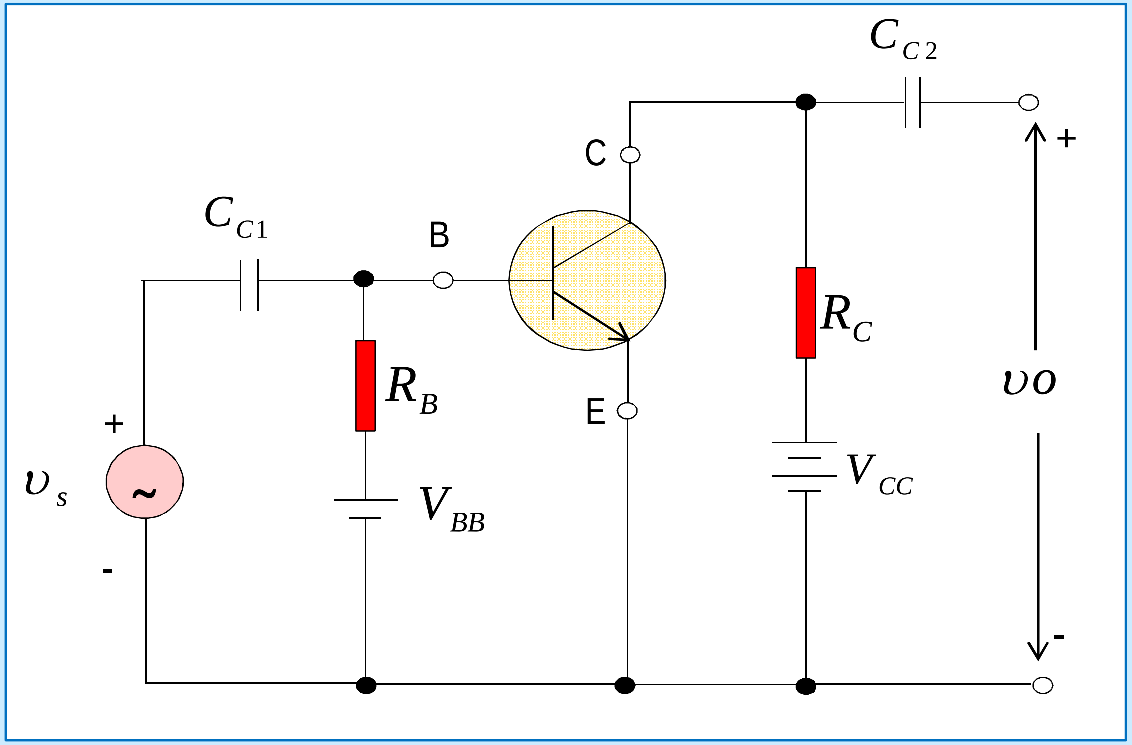
- High input resistance (~ 150 k ohm)
- Low output resistance (~ 800 ohm)
- High current gain (~100)
- Low voltage gain (less then unity)

Transistor data sheet

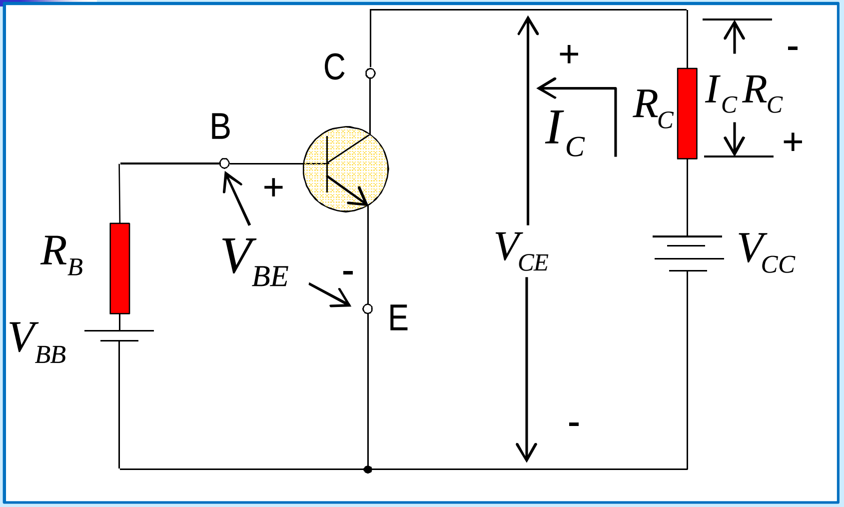
Important parameters

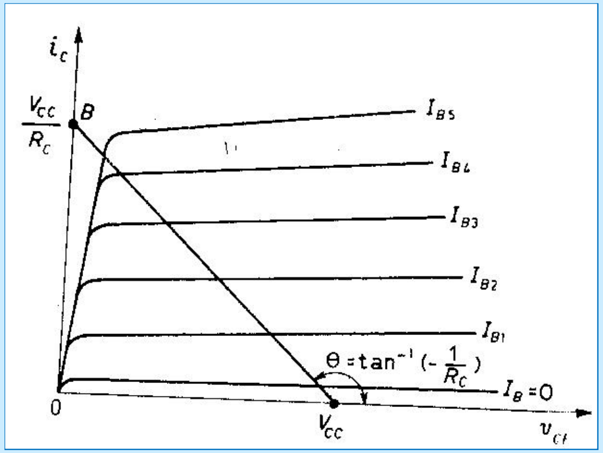
- Maximum power dissipation
- Maximum allowable voltage
- Current gain
- Max frequency of operation

Basic CE amplifier circuit



DC load line





$$V_{CC} = I_C R_C + V_{CE}$$

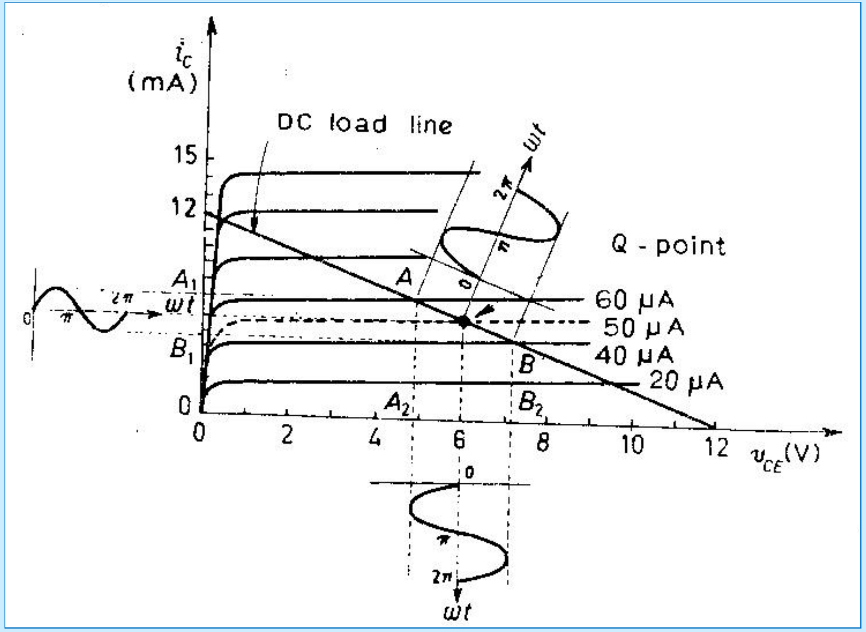
$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

$$y = mx + c$$

$$(i) V_{CE} = V_{CC}; \quad I_C = 0$$

$$(ii) V_{CE} = 0; \quad I_C = \frac{V_{CC}}{R_C}$$

Amplification and Q-point



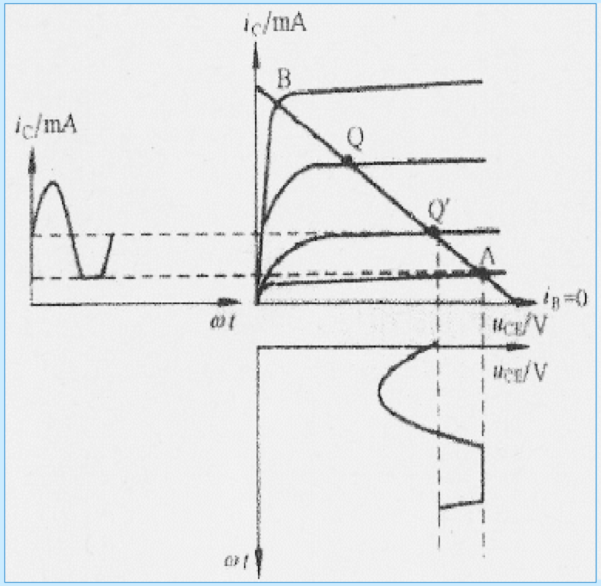
$$(i)\,Current\,gain,\; A_i = \frac{\Delta i_C}{\Delta i_B} = \frac{(7.3-4.8)10^{-3}}{(60-40)\times 10^{-6}} = 125$$

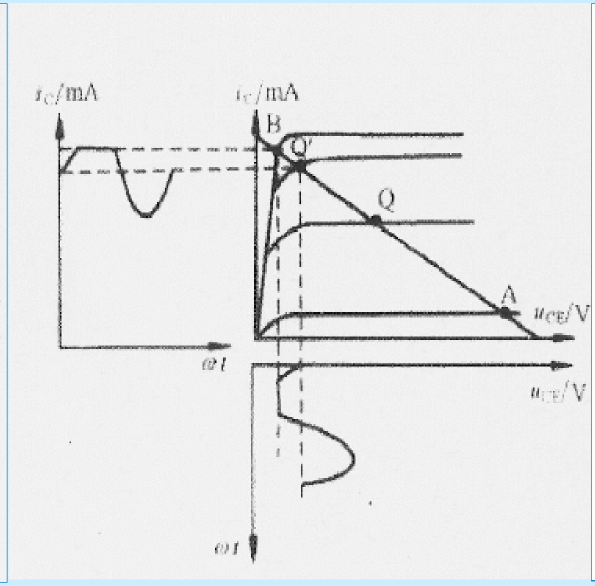
$$(ii)\,Votage\,gain,\; A_\upsilon = \frac{\Delta \upsilon_{CE}}{\Delta \upsilon_{BE}} = \frac{7.1-4.9}{20\times 10^{-3}} = 110$$

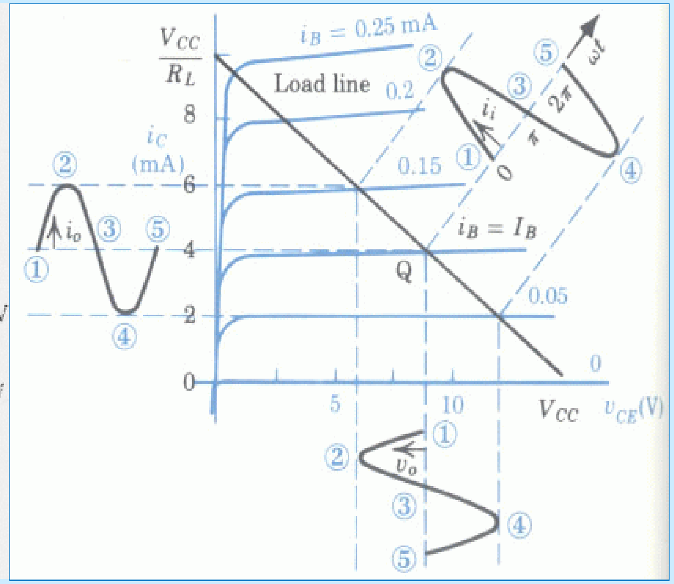
$$(iii)\,Power\,gain, = \frac{Output\,ac\,power}{input\,ac\,power} = \frac{I_c V_{ce}}{I_b V_{be}}$$

$$= A_i \times A_\upsilon = 125\times 110 = 13750$$

Selection of Q-point



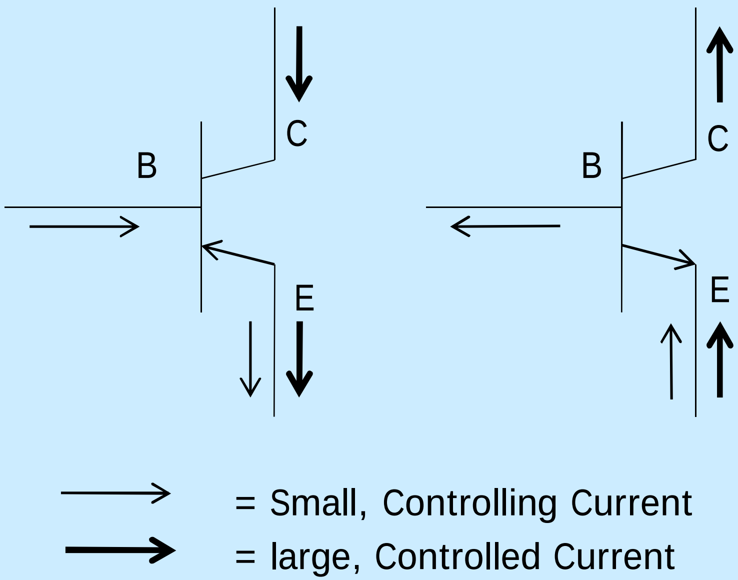




Logic Gate Using Transistor

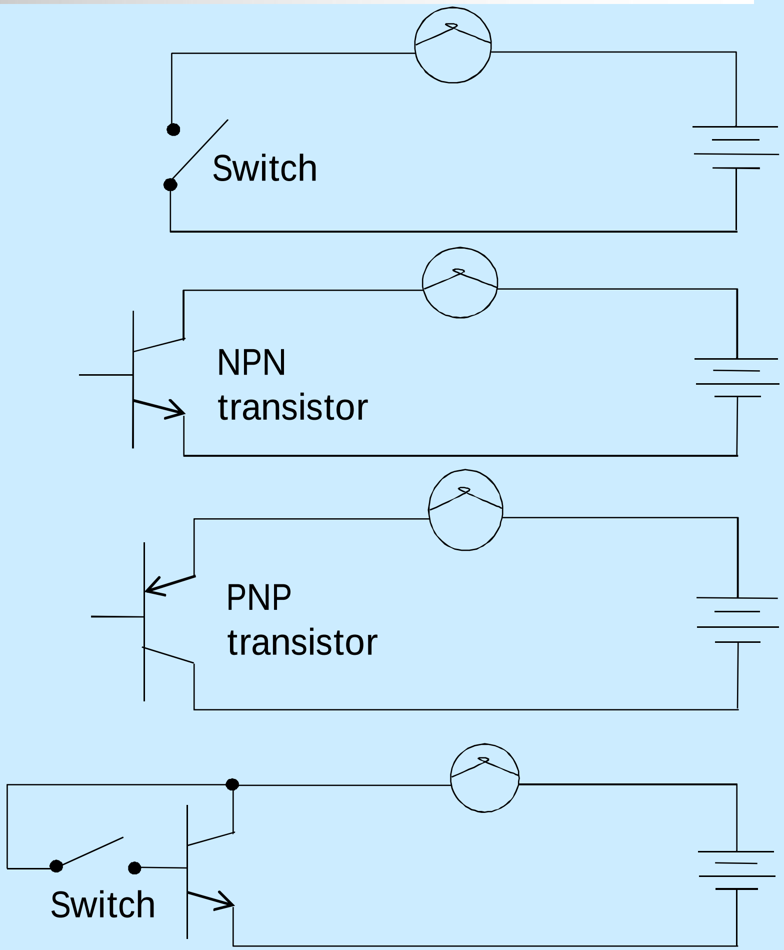
Current regulator

- Transistors function as current regulators by allowing a small current to control a larger current. The amount of current allowed between collector and emitter is primarily determined by the amount of current moving between base and emitter.
- In order for a transistor to properly function as a current regulator, the controlling (base) current and the controlled (collector) currents must be going in the proper directions: meshing additively at the emitter and going *against* the emitter arrow symbol.

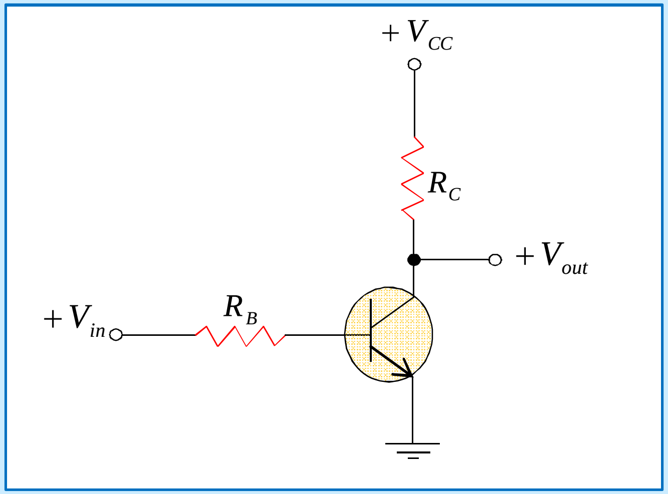


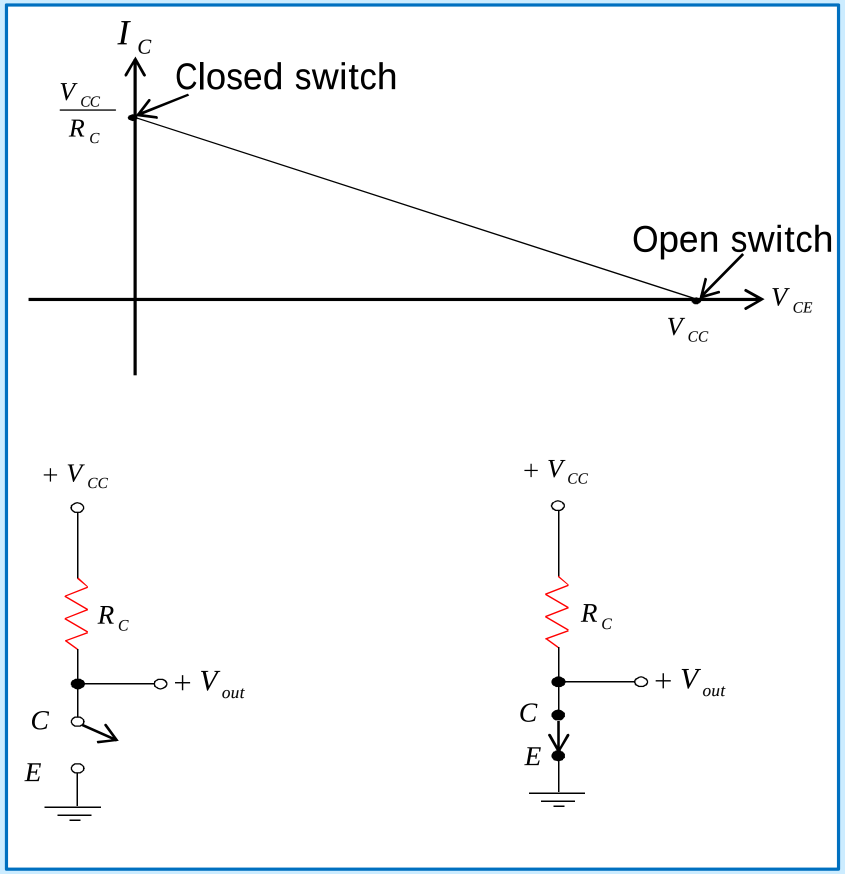
Transistor as a switch

- Transistor's collector current is proportionally limited by its base current, it can be used as a sort of current-controlled switch. A relatively small flow of electrons sent through the base of the transistor has the ability to exert control over a much larger flow of electrons through the collector
- When a transistor has zero current through it, it is said to be in a state of *cutoff*
- When a transistor has maximum current through it, it is said to be in a state of *saturation.*



Inverter





$$I_C = \beta_{dc} I_B$$

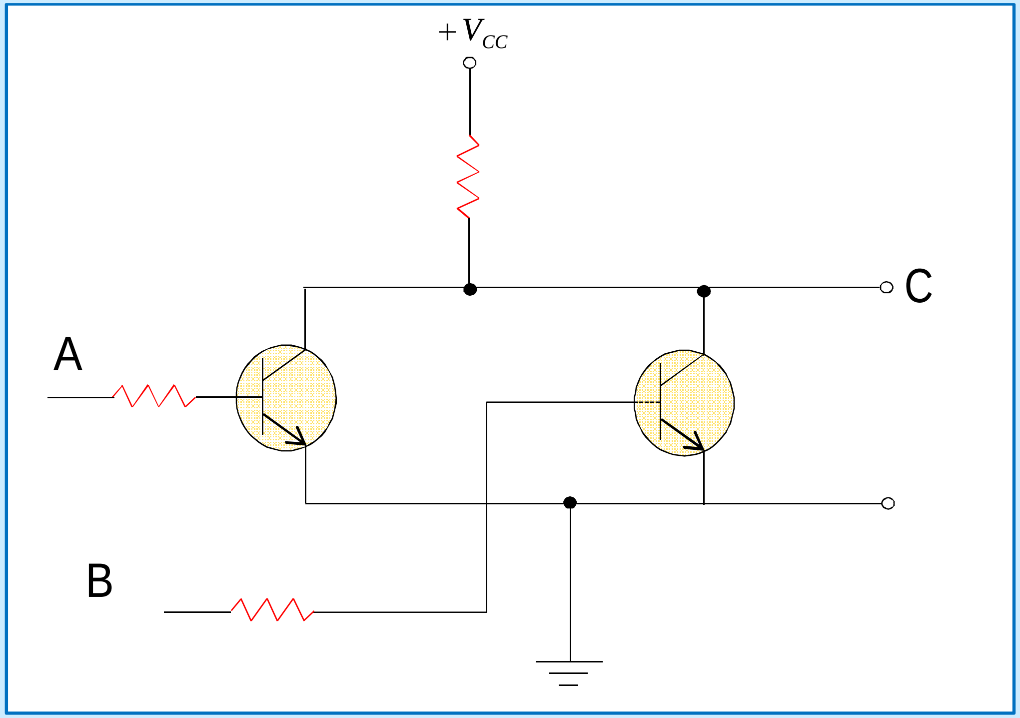
$$I_B = \frac{V_{in} - V_{BE}}{R_B}$$

$$V_{out} = V_{CC} - I_C R_C$$

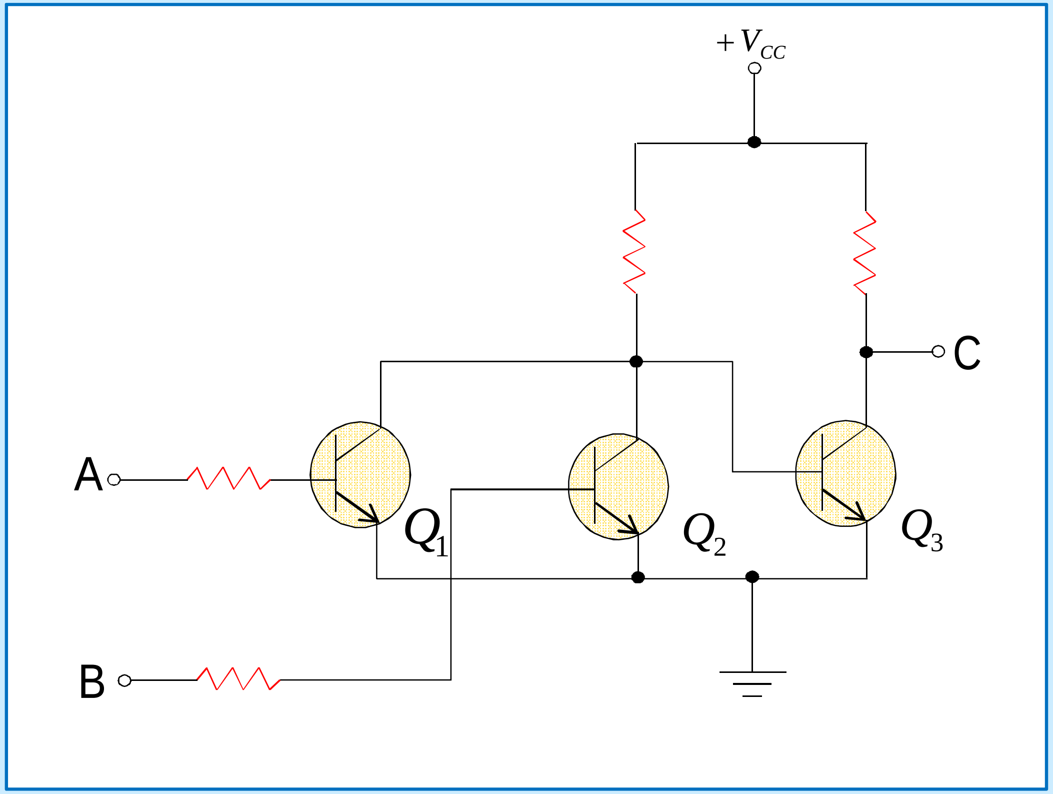
0 input = open switch = output 1

1 input = close circuit = output 0

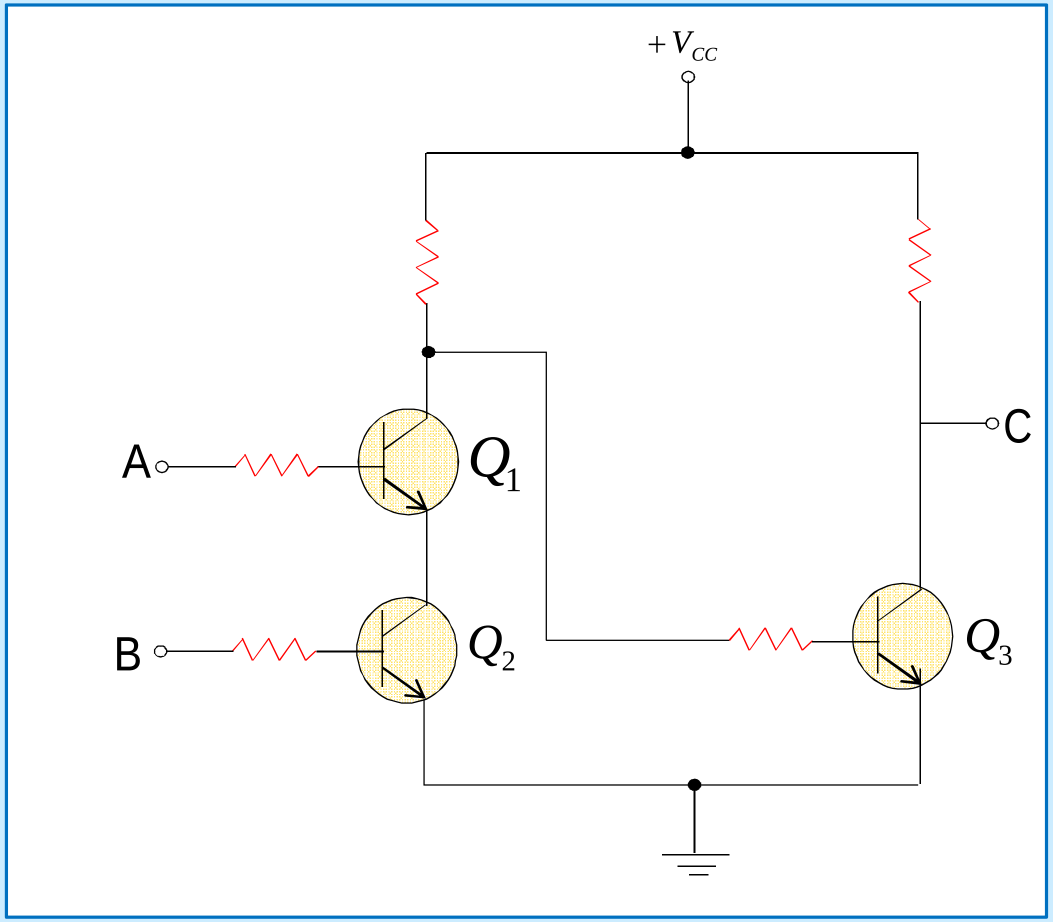
NOR Gate



OR Gate



AND Gate



NAND Gate

XOR Gate

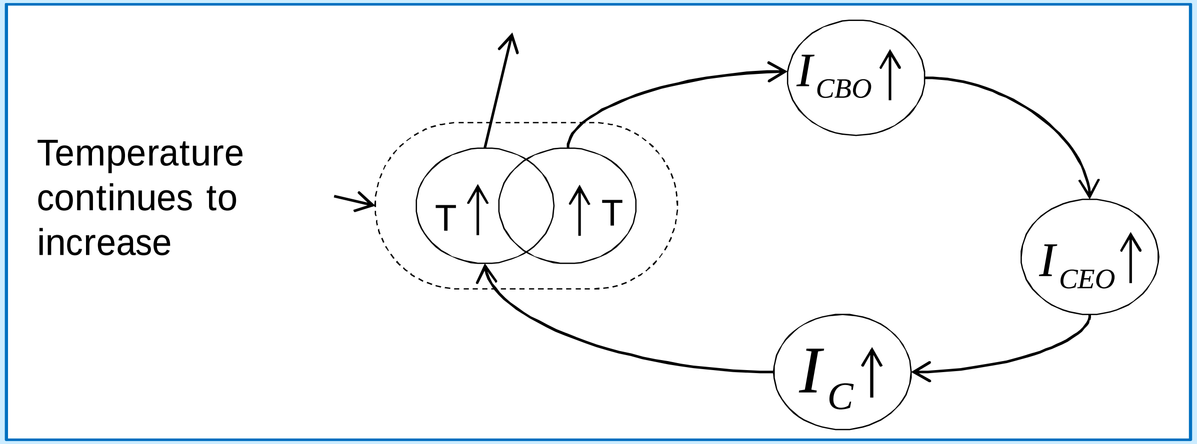
Transistor Biasing Circuit

Stabilization of Q-point

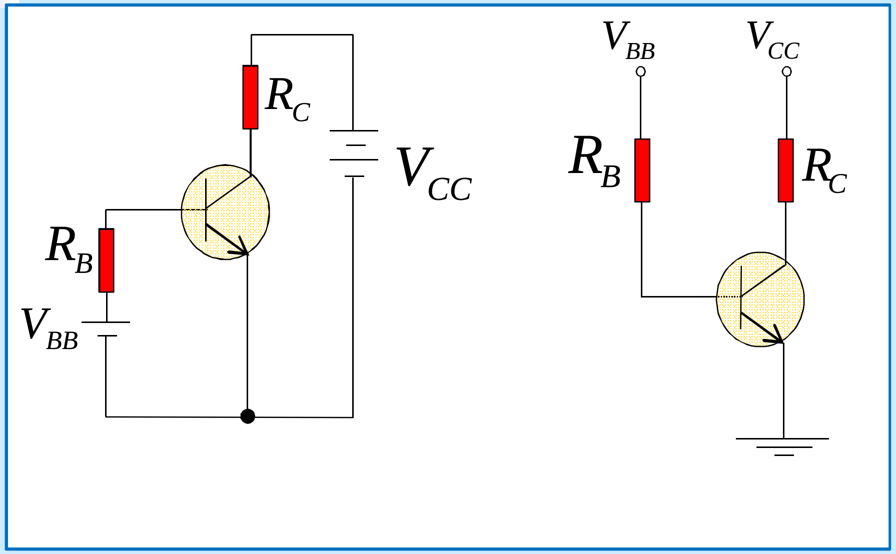
Requirement of biasing circuit

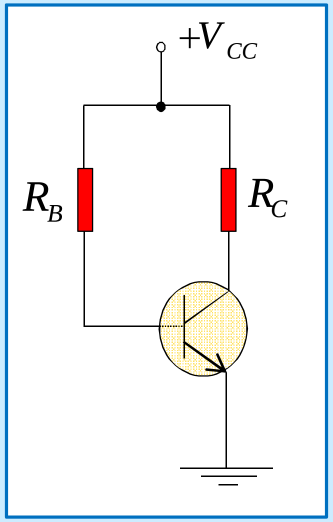
- Operating point in the centre of active region
- Stabilization of collector current against temperature variations
- Making operating point independent of transistor parameters

Different biasing techniques used for achieving these points



Fixed Bias





$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$I_C = \beta I_B + I_{CEO}$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C \leq \frac{V_{CC}}{R_C}$$

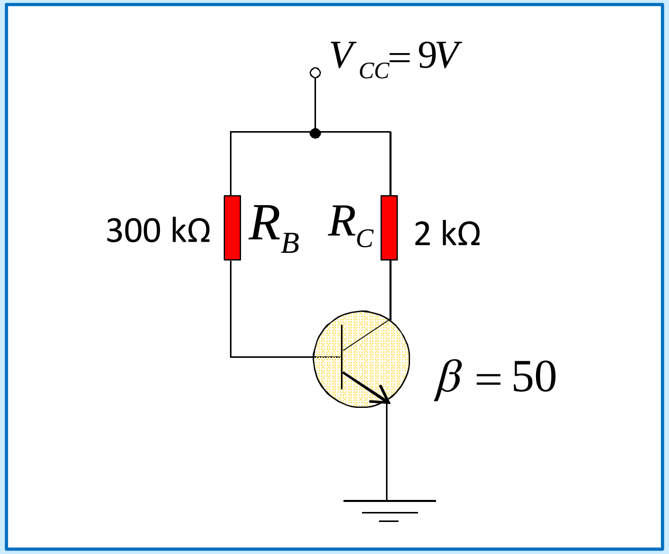
$$I_{C(Sat)} = \frac{V_{CC}}{R_C}$$

Steps for calculating Q-point in fixed bias

1. Calculate base voltage, in case V_{BE} is known, use more accurate calculation.
2. Calculate collector current from base current, make sure its not greater than $I_{c(sat)}$
3. Calculate collector-emitter voltage

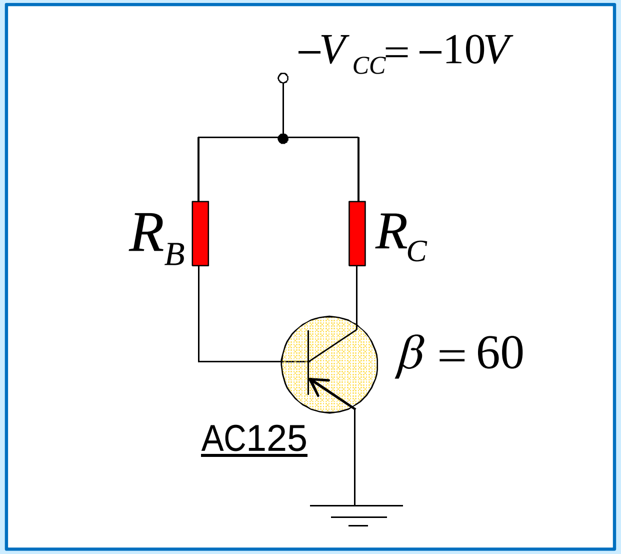
Problem

- Calculate the Q-point for the circuit given in figure



Problem

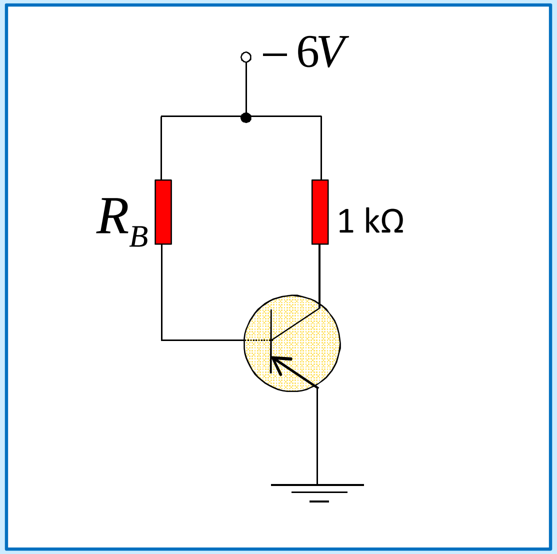
- Calculate
  - Q-point in circuit. Given R_C=1 k ohm and R_B=100 k ohm
  - If transistor is replaced by another unit of beta=150 instead of 60. Determine its new Q-point.



Assignment (1 Mark)

In a given circuit, a supply of 6 V and a load resistance of 1 k ohm is used.

- Find the value of resistance R_B so that a germanium transistor with β=20 and I_{CBO}=2uA draws an I_C of 1 mA.
- What Ic is drawn if the transistor parameters change to β=25 and I_{CBO} = 10 uA due to rise in temperature ?



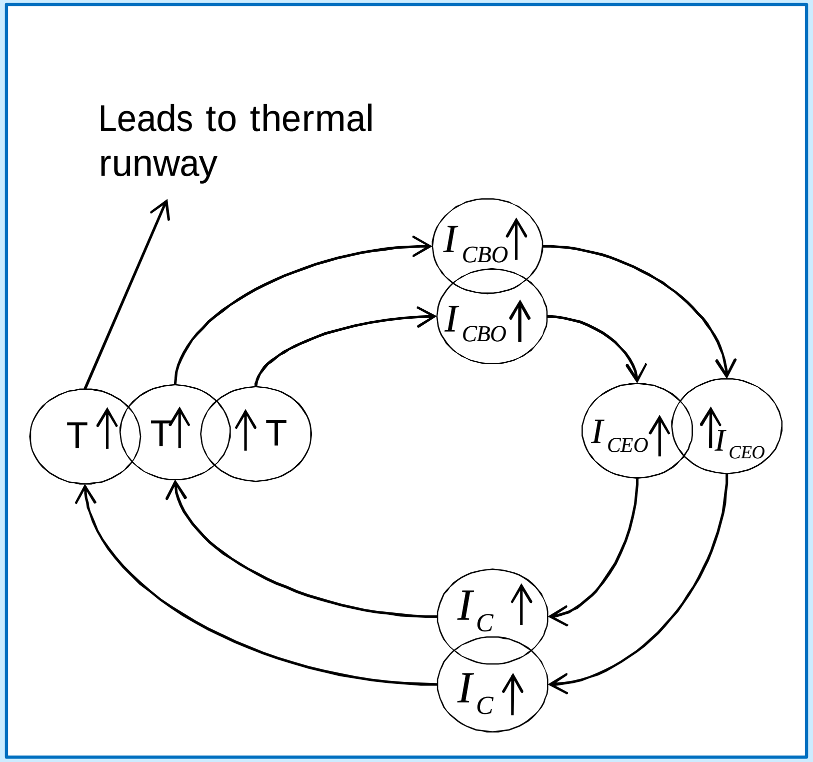
Fixed bias features

Advantages

- Very simple
- very few component
- Easy to fix Q point by changing R_B

Limitations

- Thermal runway
- Strongly β dependent Q-point



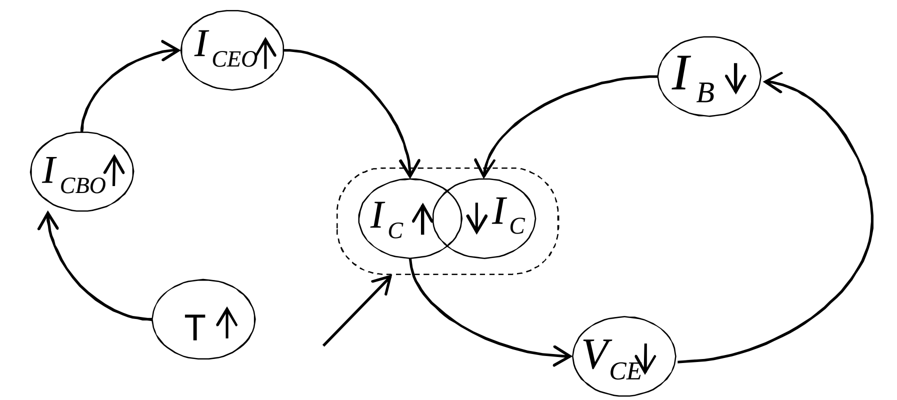
Collector to base bias circuit

$$V_{CC} = R_C(I_C + I_B) + I_B R_B + V_{BE}$$

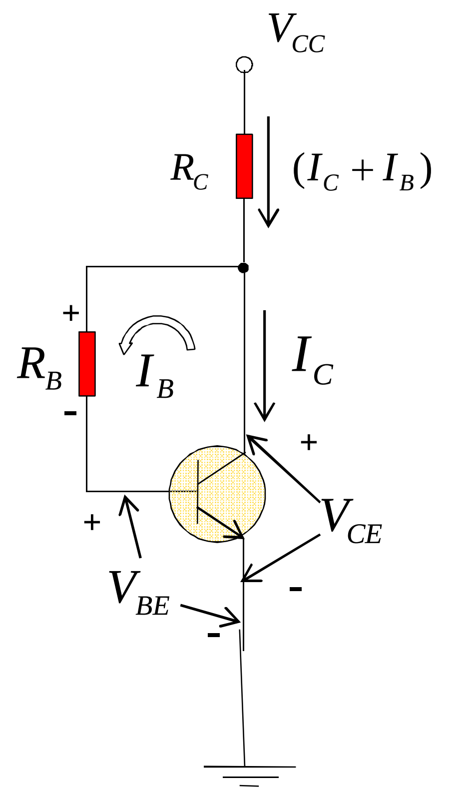
$$V_{CC} = R_C I_C + (R_C + R_B) I_B + V_{BE}$$

$$I_B = \frac{(V_{CC} - I_C R_C) - V_{BE}}{R_C + R_B}$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_C + R_B}$$



Rising tendency is checked



Contd.

$$V_{CC} = R_C \beta I_B + (R_C + R_B) I_B + V_{BE}$$

$$V_{CC} = V_{BE} + [R_B + (\beta + 1) R_C] I_B$$

$I_B \sim Vcc/(R_B+\beta Rc)$

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C \cong V_{CC} - I_C R_C$$

Shift in Q-point due to change in β is not much as it occurs in case of fixed bias

Features of collector to base bias circuit

Advantages

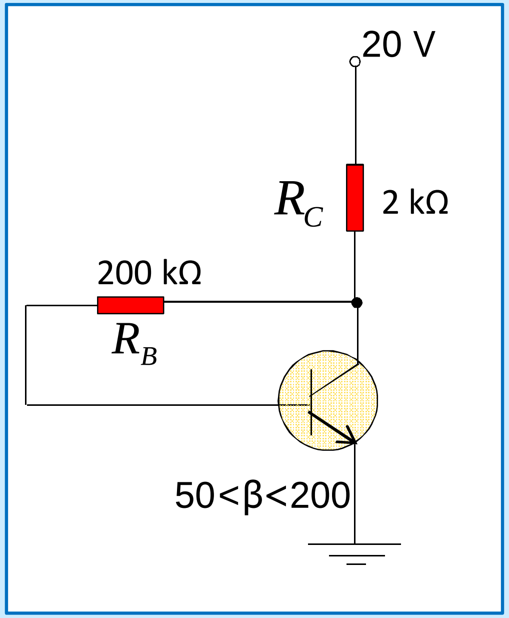
- Check thermal runway
- Q-point less dependent on β value

Limitations

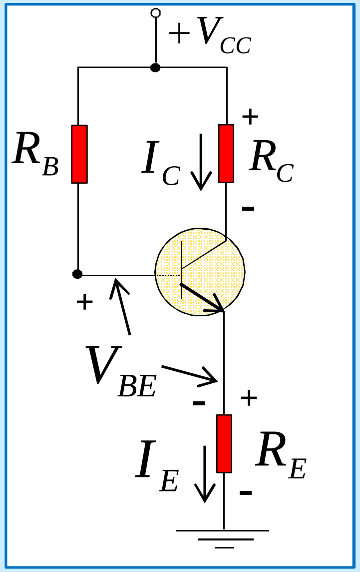
- Base resistance also provide AC feedback, that reduce voltage gain

Problem

Calculate the minimum and maximum collector current in the given circuit, if β varied with in the limit indicated.



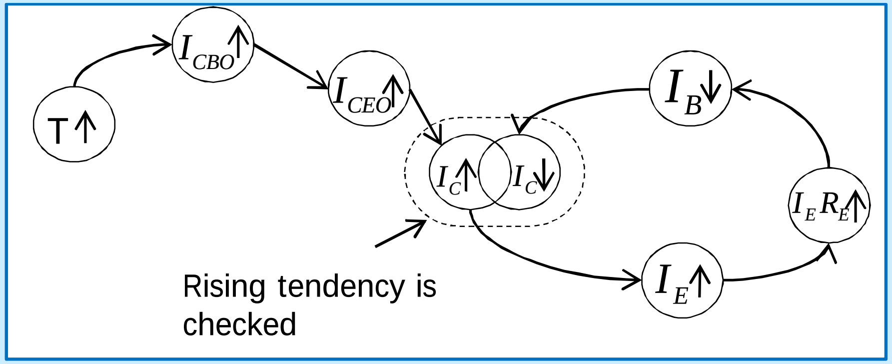
Bias circuit with emitter resistance

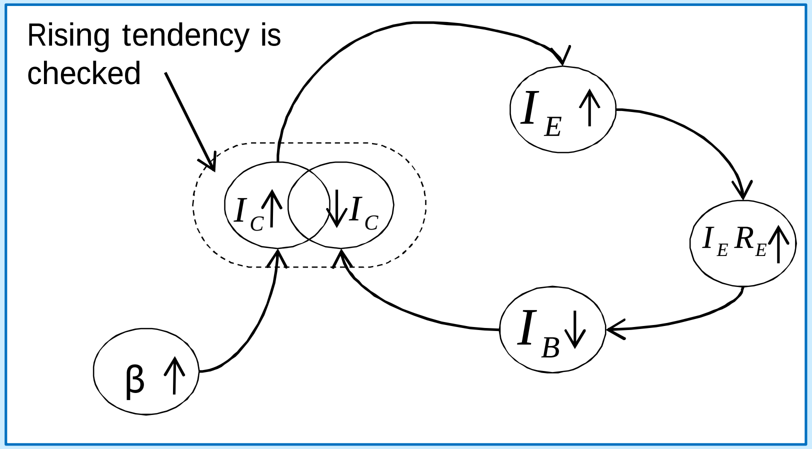


$$V_{CC} = R_B I_B + V_{BE} + I_E R_E$$

$$I_B = \frac{(V_{CC} - I_E R_E - V_{BE})}{R_B}$$

$$I_B \cong \frac{(V_{CC} - I_E R_E)}{R_B}$$





Contd.

$$\boxed{V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \cong \frac{V_{CC}}{R_B + \beta R_E}}$$

$$\boxed{I_C = \beta I_B = \frac{\beta V_{CC}}{R_B + \beta R_E} = \frac{V_{CC}}{R_E + (R_B / \beta)}}$$

$$\boxed{V_{CC} = I_C R_C + V_{CE} + I_E R_E}$$

$$\boxed{V_{CE} = V_{CC} - (R_C + R_E) I_C}$$

Features of bias circuit with emitter resistance

Advantages

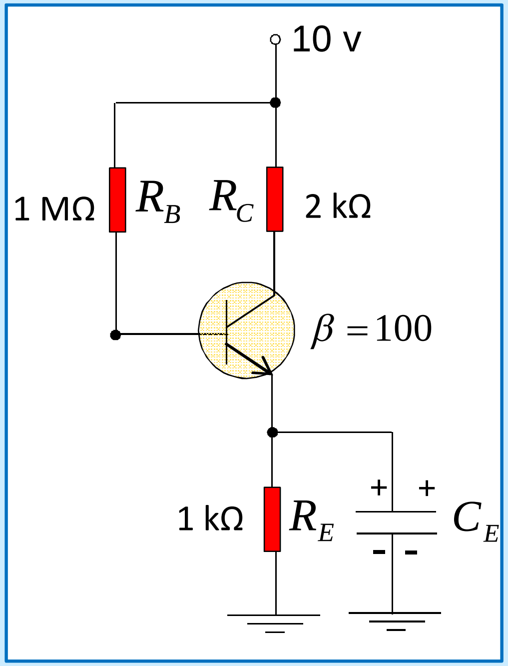
- Provide good stabilization of Q-point against temperature and β variation

Limitations

- Emitter resistance provide a feedback causes reduction in voltage gain.
- For getting very good stabilization

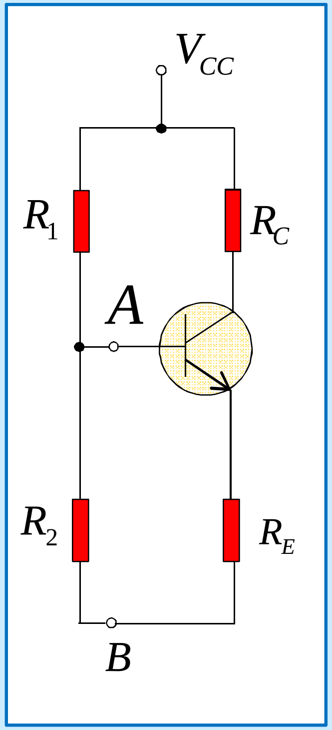
$$R_E >> \frac{R_B}{\beta}$$

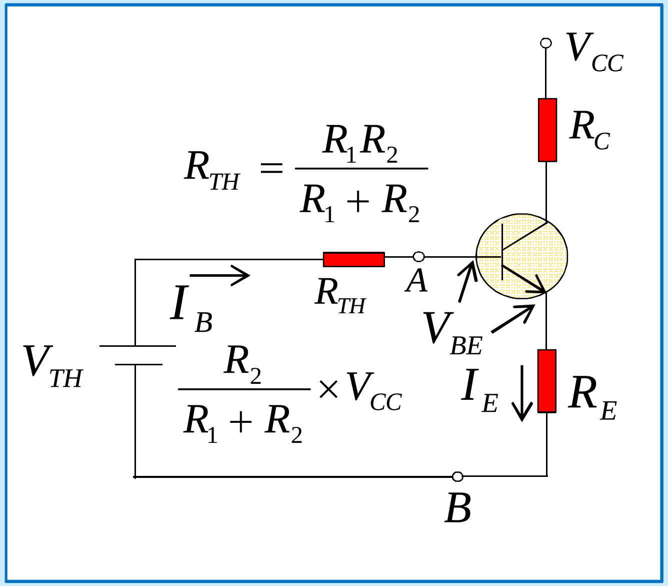
  - For large R_E, high DC source is required
  - For small RB, low DC source is required

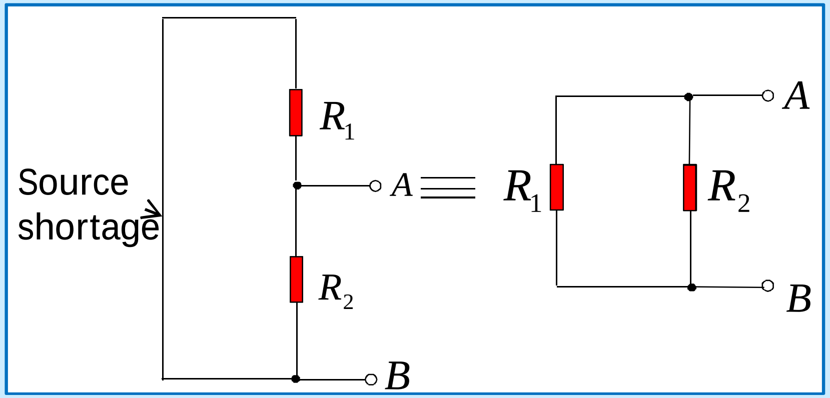


Problem: Calculate values of 3 currents

Voltage divider biasing circuit







$$V_{TH} = I_B R_{TH} + V_{BE} + R_E I_E$$

$$V_{TH} = I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E$$

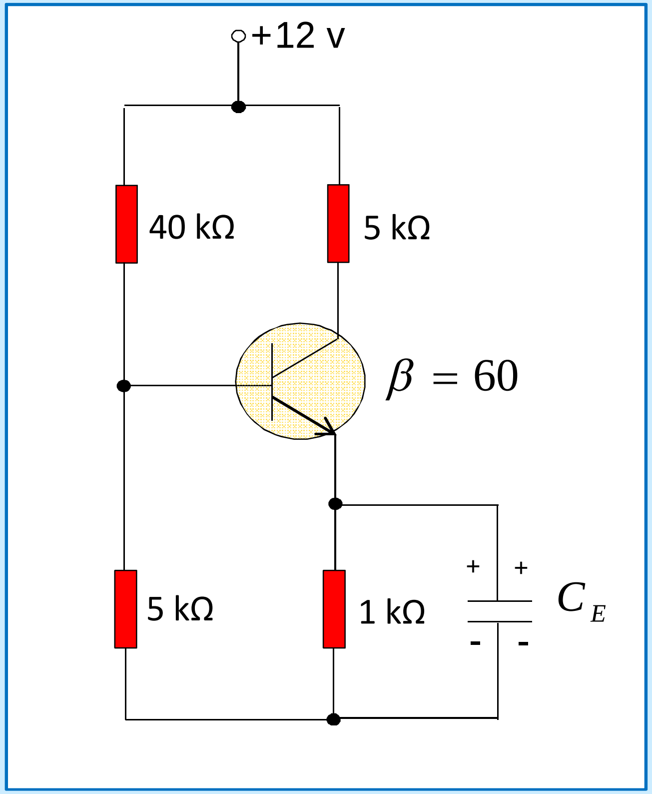
$$I_B [R_{TH} + (\beta + 1) R_E] = V_{TH} - V_{BE}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E} \cong \frac{V_{TH}}{R_{TH} + \beta R_E}$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

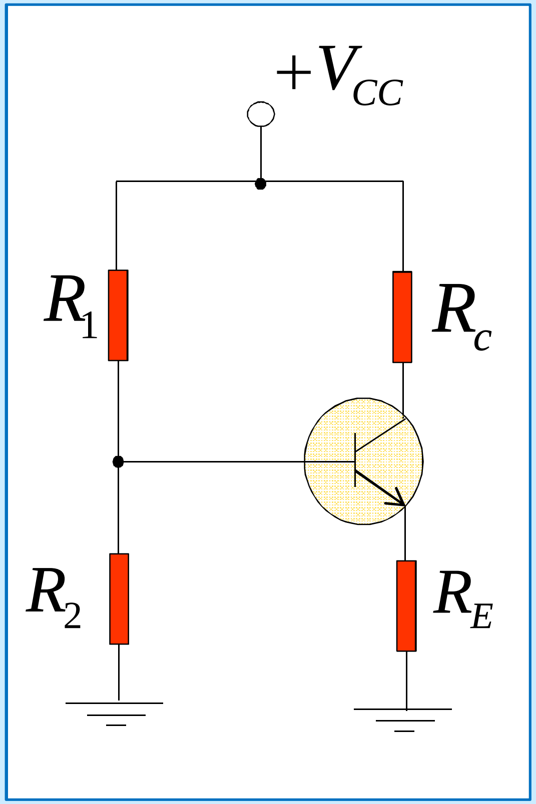
Problem

- Find Q point



Amplifiers

DC Behavior

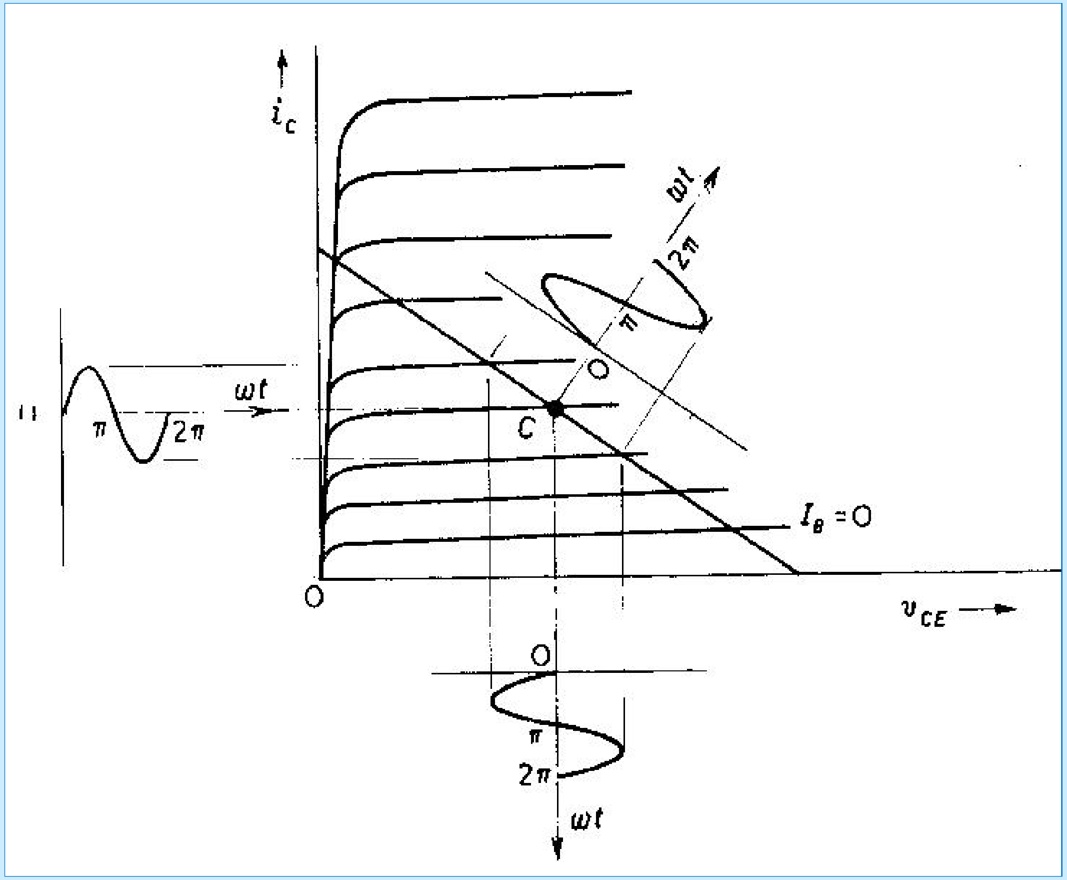


$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

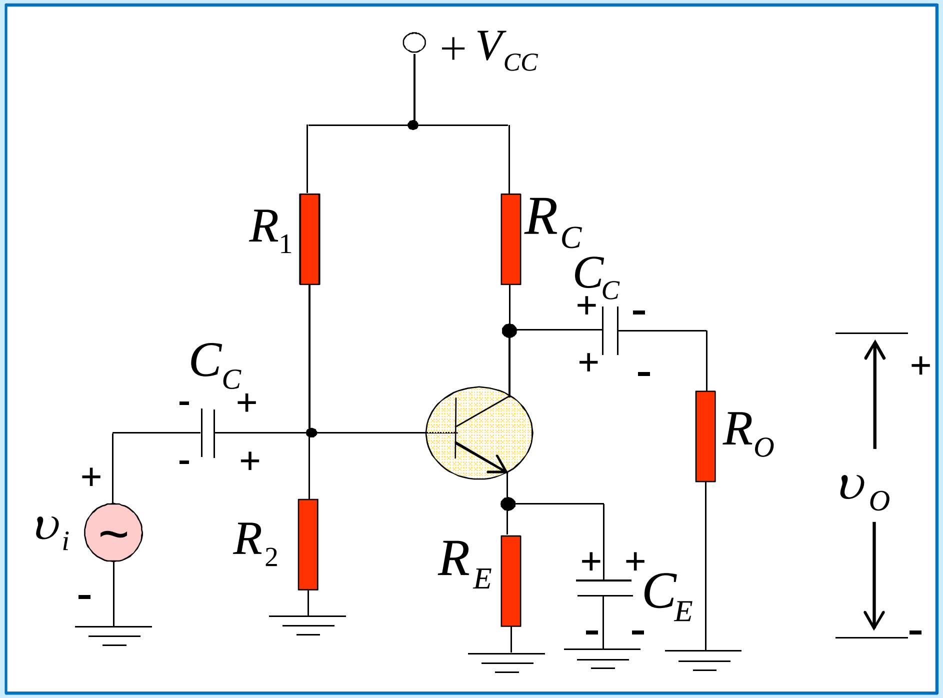
$$= V_{CE} + I_C (R_C + R_E)$$

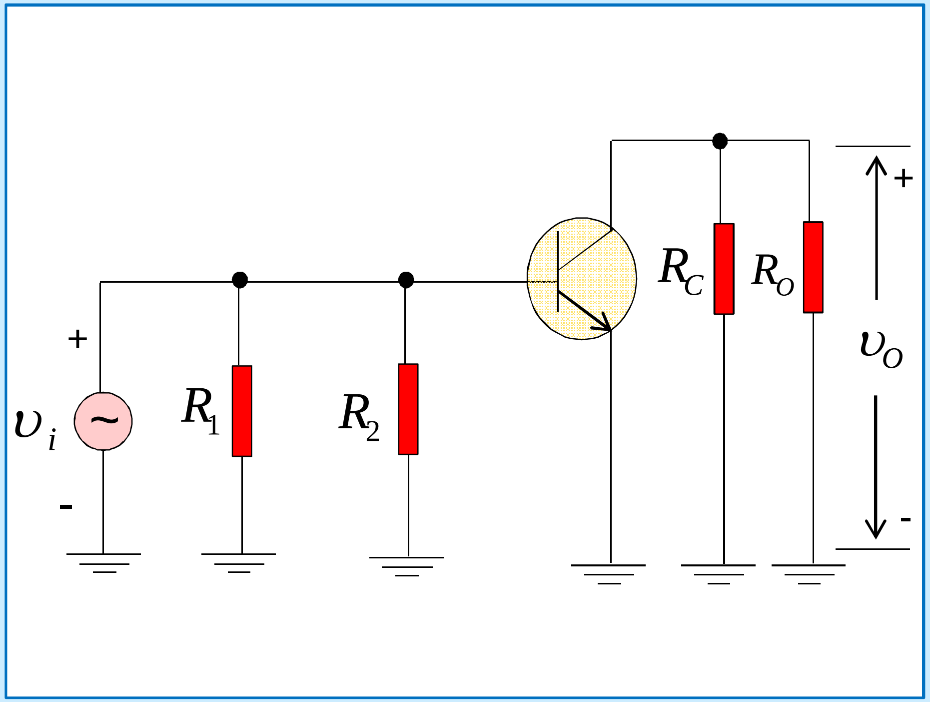
$$I_C = \frac{-1}{(R_C + R_E)} V_{CE} + \frac{V_{CC}}{(R_C + R_E)}$$

Input and Output phase



AC Behavior

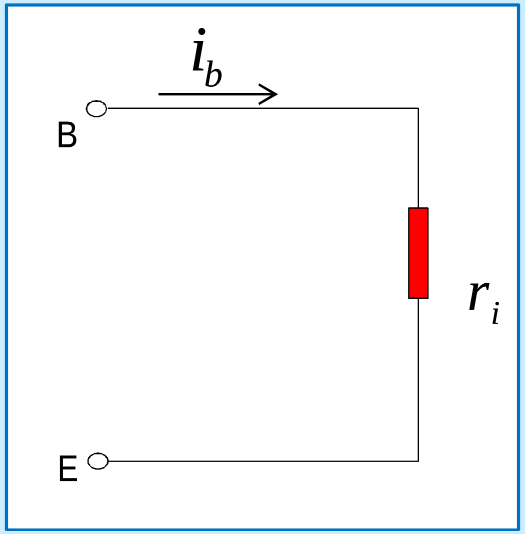




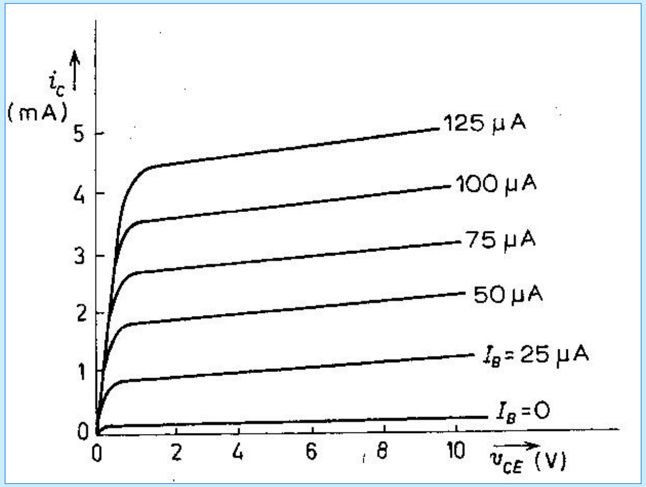
AC equivalent

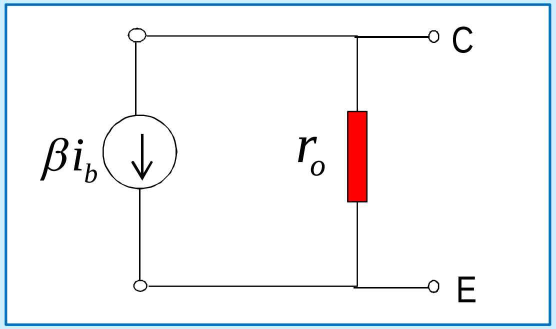
Transistor Equivalent Circuit

- Input



- Output





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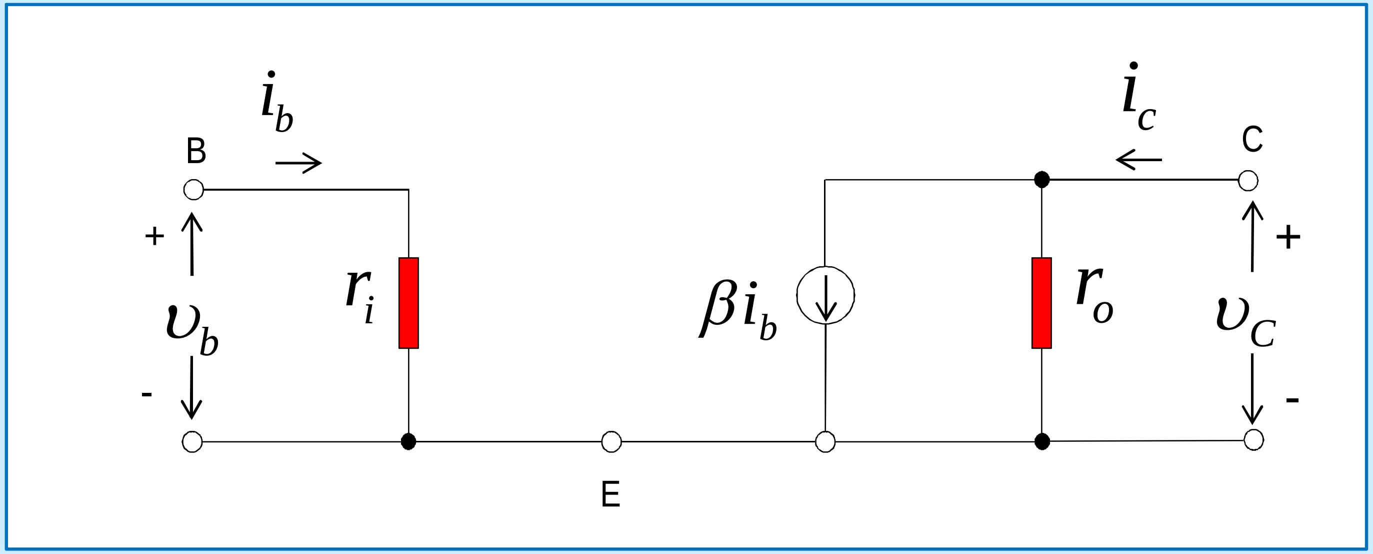
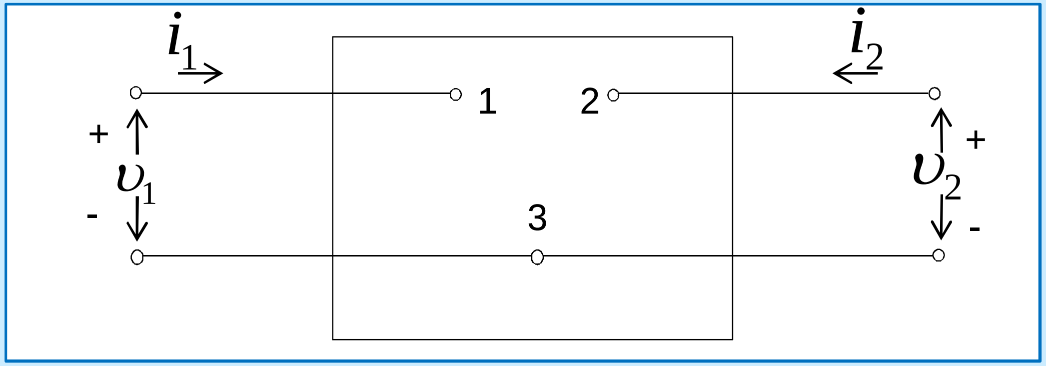


h-Parameter

- Manufacture specify characteristics of a transistor in terms of *h* (hybrid) parameters
- Hybrid is used with these parameters because they are a mixture of constants having different units
- It becomes popular because they can be measure easily

Transistor as two-port network



$$\upsilon_1 = h_{11} i_1 + h_{12} \upsilon_2$$

$$i_2 = h_{21} i_1 + h_{22} \upsilon_2$$

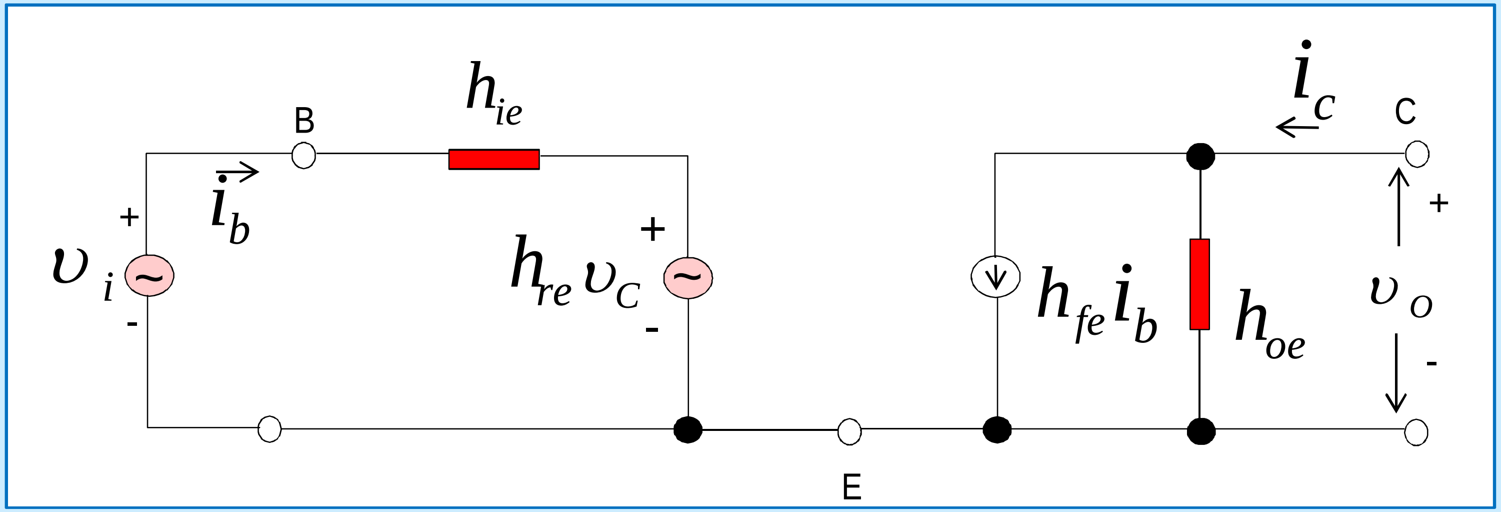
$h_{11} = \left.\dfrac{\upsilon_1}{i_1}\right|_{\upsilon_2 = 0}$ = Input impedance (with output shorted) = h_i

$h_{21} = \left.\dfrac{i_2}{i_1}\right|_{\upsilon_2 = 0}$ = Forward Current ratio (with output shorted) = h_f

$h_{12} = \left.\dfrac{\upsilon_1}{\upsilon_2}\right|_{i_1 = 0}$ = Reverse voltage ratio (with input open) = h_r

$h_{22} = \left.\dfrac{i_2}{\upsilon_2}\right|_{i_1 = 0}$ = Output admittance (with input open) = h_o

Hybrid equivalent circuit



$h_{ie} = r_i$, dynamic input resistance

$h_{fe} = \beta$, current amplification factor

$1/h_{oe} = r_o$, dynamic output resistance.

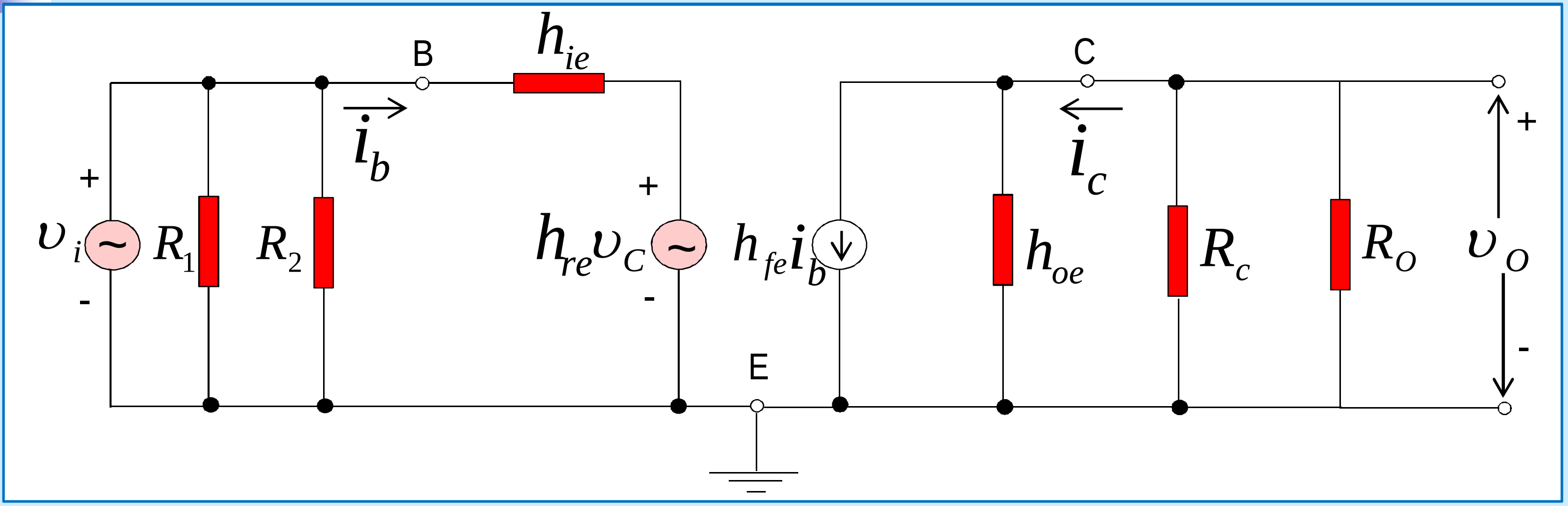
$h_{ie} =$ 1 kΩ

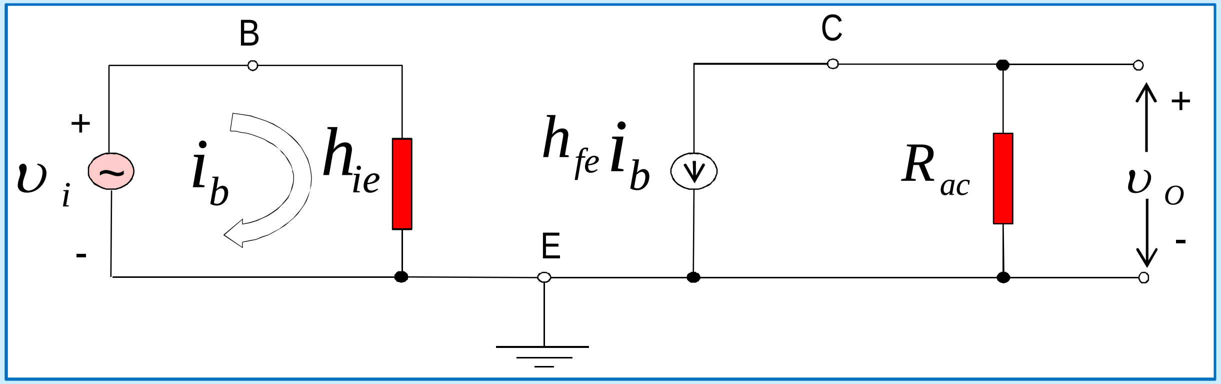
$h_{re} = 2.5\times10^{-4}$

$h_{fe} = 50$

$h_{oe} =$ 25 μs (or, $1/h_{oe} =$ 40 kΩ)

Amplifier analysis





$$R_{ac} = R_C \parallel R_O = \frac{R_C R_O}{R_C + R_O}$$

Contd.

$$Current\ \ gain,\ A_i = \frac{Output\ \ Current}{Input\ Current} = \frac{i_c}{i_b}$$

$$= \frac{h_{fe} i_b}{i_b} = h_{fe}$$

$$A_i = \beta$$

$$Voltage\ \ gain,\ A_\upsilon = \frac{Output\ \ Voltage}{Input\ Voltage} = \frac{-h_{fe} i_b R_{ac}}{i_b h_{ie}}$$

$$= \frac{-h_{fe} R_{ac}}{h_{ie}}$$

$$A_\upsilon = \frac{\beta R_{ac}}{r_i} \angle 180^0$$

$$A_p = A_i A_\upsilon$$

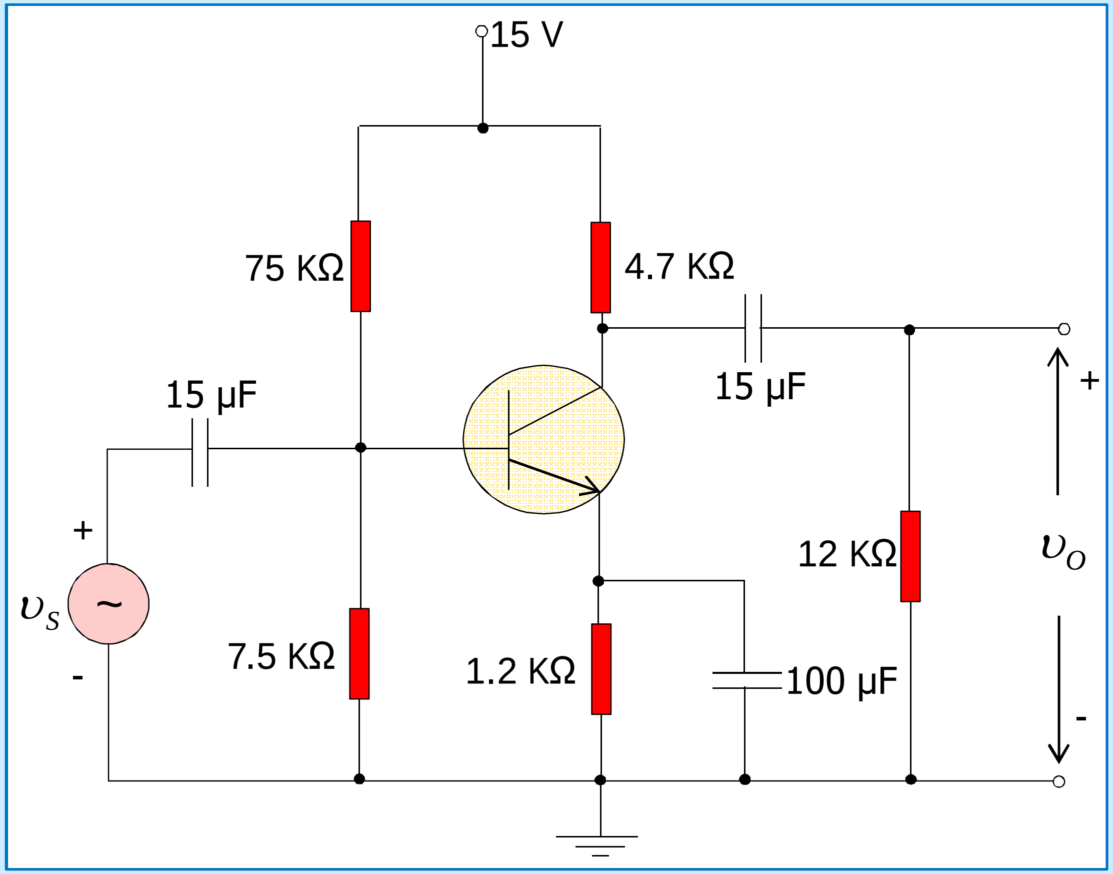
$$Z'_{in} = R_1 \parallel R_2 \parallel h_{ie} \cong h_{ie}$$

$$Z'_o = (1/h_{oe}) \parallel R_{ac} \cong R_{ac}$$

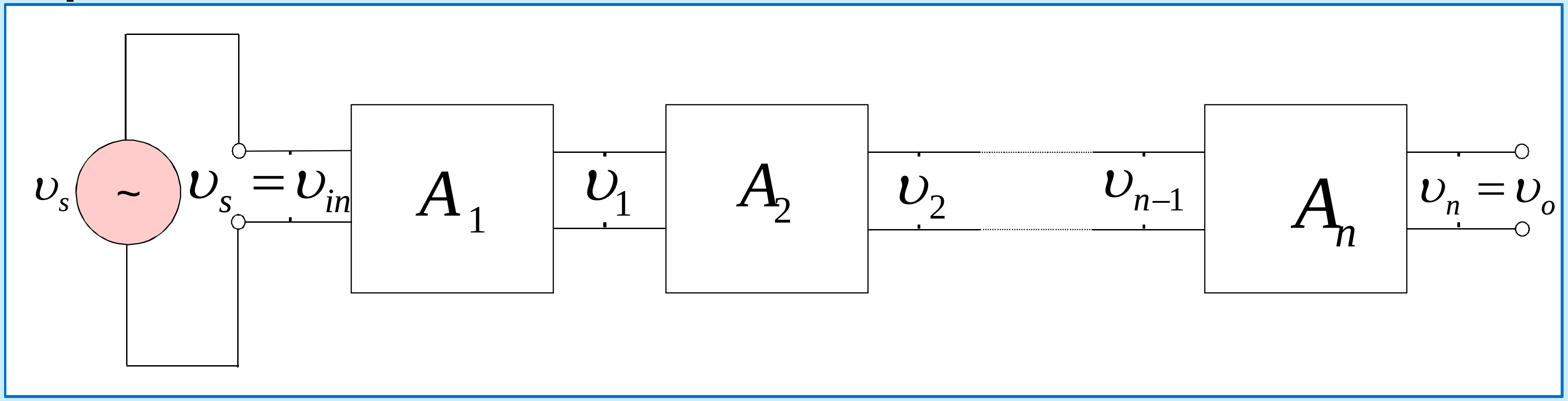
Problem

Current Gain 150, R_{in}=2 k ohm

Calculate voltage gain and input impedance



Multi-stage Amplifiers



$$A = \frac{\upsilon_o}{\upsilon_s} = \frac{\upsilon_1}{\upsilon_s} \times \frac{\upsilon_2}{\upsilon_1} \times \ldots \times \frac{\upsilon_{n-1}}{\upsilon_{n-2}} \times \frac{\upsilon_o}{\upsilon_{n-1}}$$

$$A = A_1 \times A_2 \times \ldots \times A_{n-1} \times A_n$$

Numbers of bels = $Log10\frac{P2}{P1}$

Contd.

$$\text{Number of dB} = 10 \times \text{Number of bels} = 10 \log_{10} \frac{P_2}{P_1}$$

$$\text{Gain in dB} = 20 \log_{10} \frac{V_2}{V_1}$$

$$A_{dB} = A_{dB1} + A_{dB2} + \ldots + A_{dBn}$$

Why dB

- Simple addition of gain
- Permits us to denote very small and very large value
- Our hearing power in logarithmic

Coupling of two stages

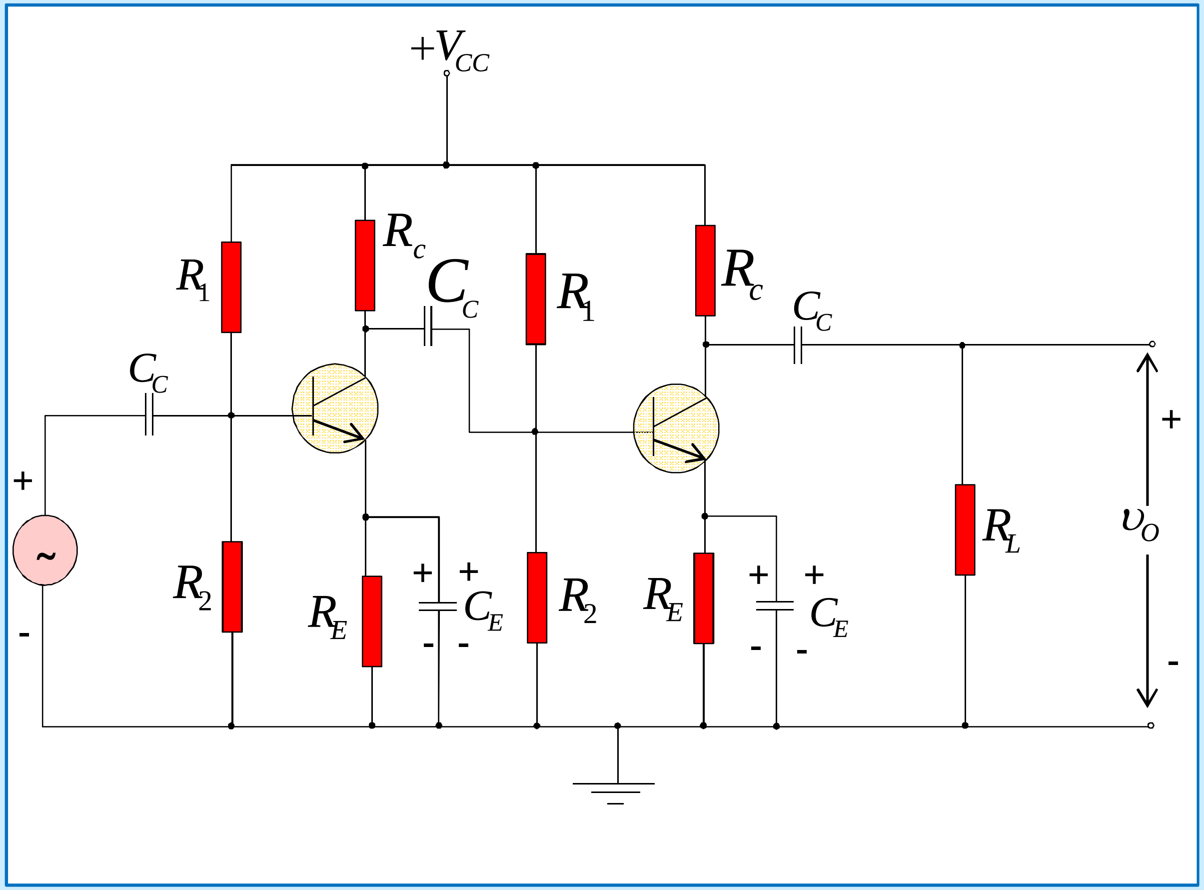
- Minimum loss of signal
- Should not affect biasing of other stage

Typical Couplings

- RC coupling
- Transformer coupling
- Direct coupling

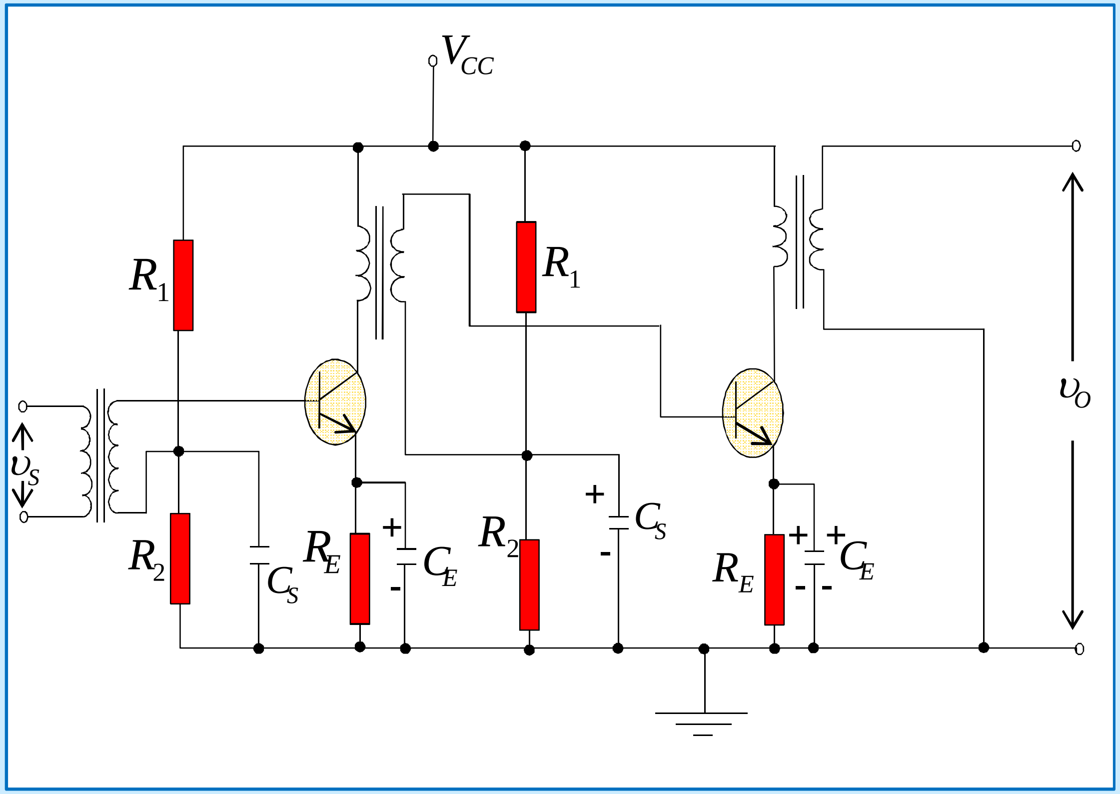
RC coupling

- Widely used
- Makes DC biasing independent
- Not good for low frequency applications



Transformer coupling

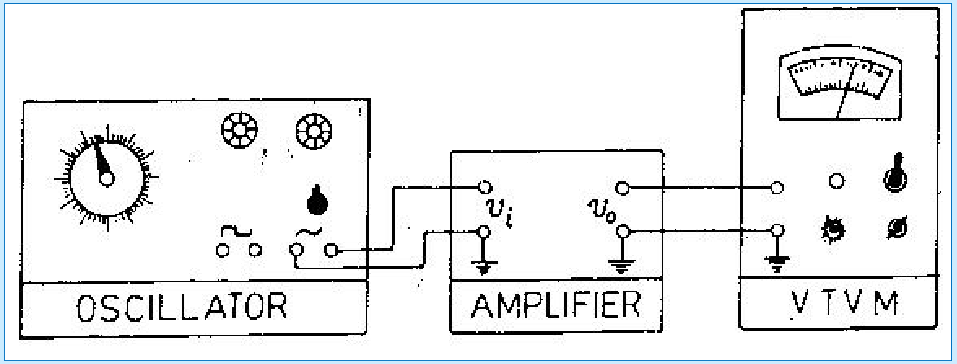
- DC isolation provided by transformer
- Bigger in size
- Does not amplify signals of different frequency equally
- Suited for power amplifiers and tuned voltage amplifiers

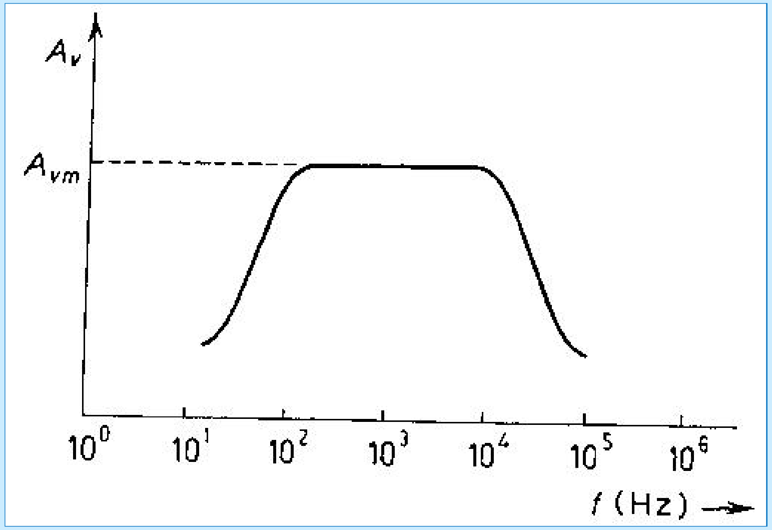


Direct coupling

- Required at very low frequency
- Affect biasing of other stage (consider this while designing)

Frequency response of Amplifier

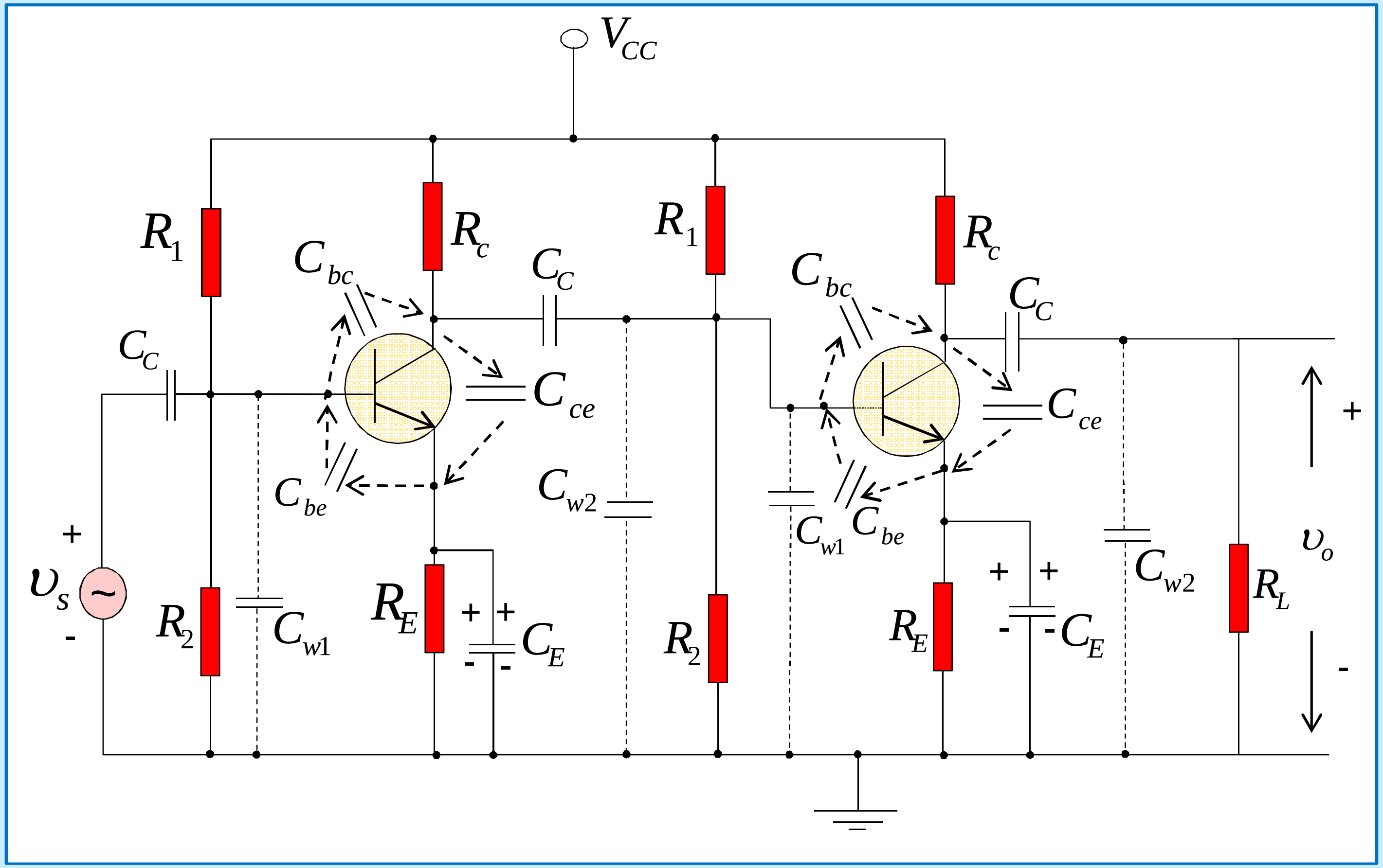




At low *f*

- Provide low gain due to high reactance of coupling capacitors

At high f



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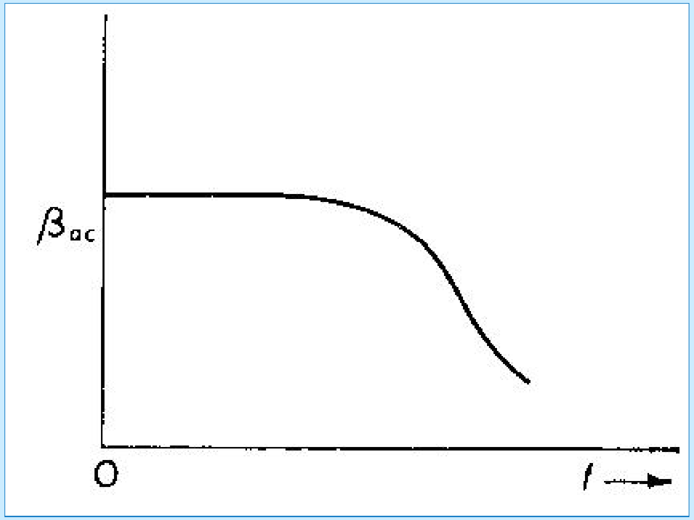
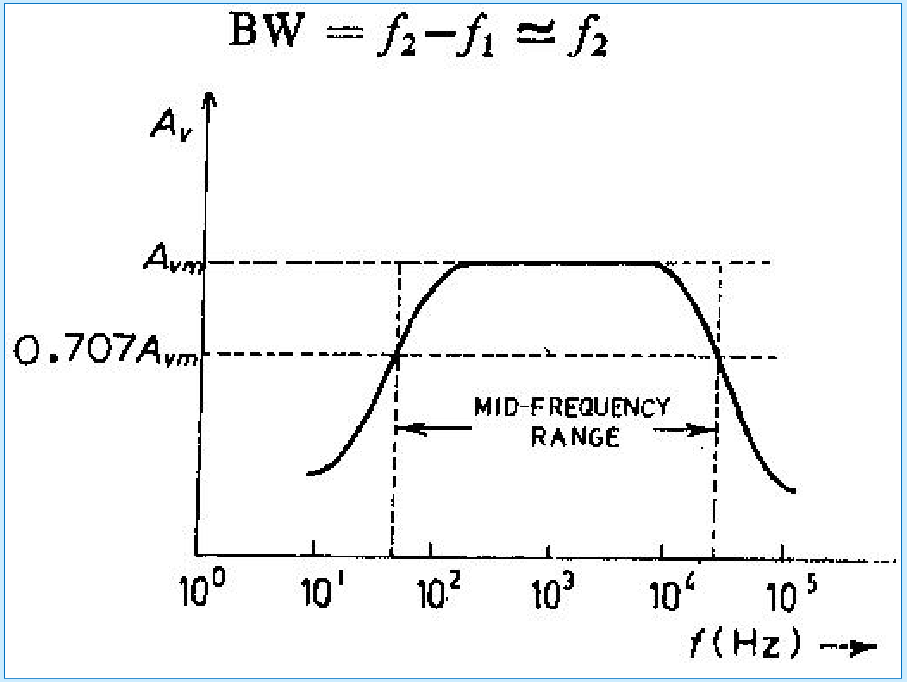


Bandwidth



$$0.707\ A_{\upsilon m} = 1/\sqrt{2}\,A_{\upsilon m}$$

Effect on band width with no. of stages

- Bandwidth decreases with increase in no. of stages
  - Because greater no. of capacitor in the circuit
- Voltage gain

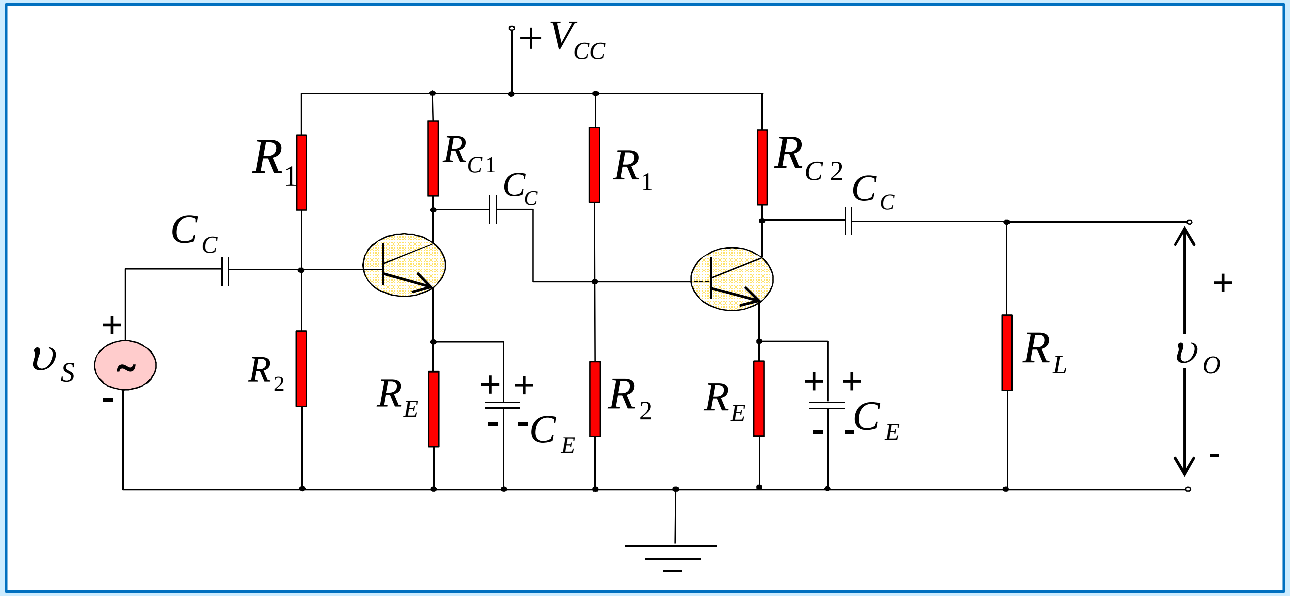
$$A'_{\upsilon} = (A_{\upsilon m})^n$$

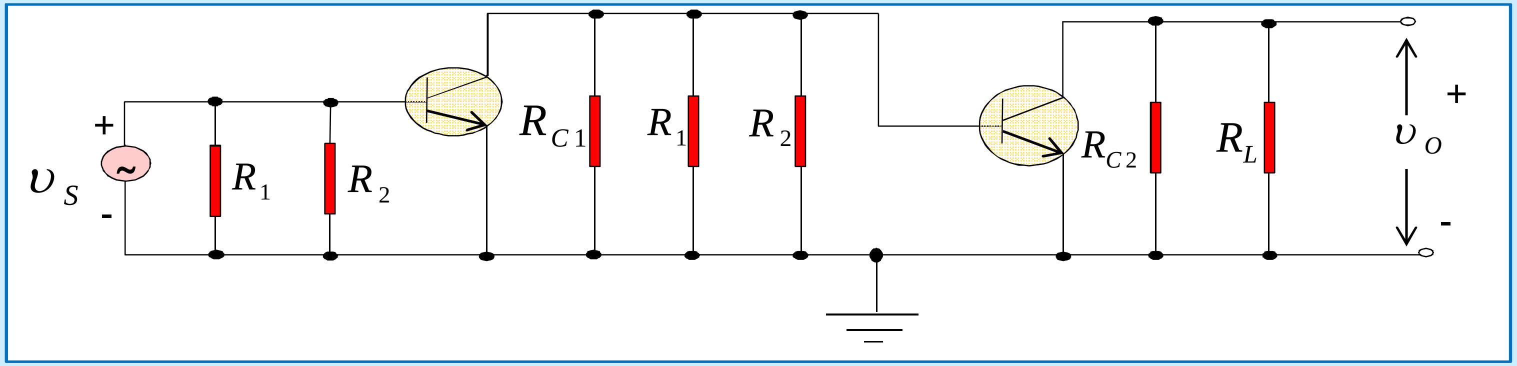
- Upper and lower cut of frequency

$$f'1 = \frac{1}{\sqrt{(2^{1/n} - 1)}} f1$$

$$f'2 = \sqrt{(2^{1/n} - 1)}\ f2$$

Two-stage RC-coupled amplifier





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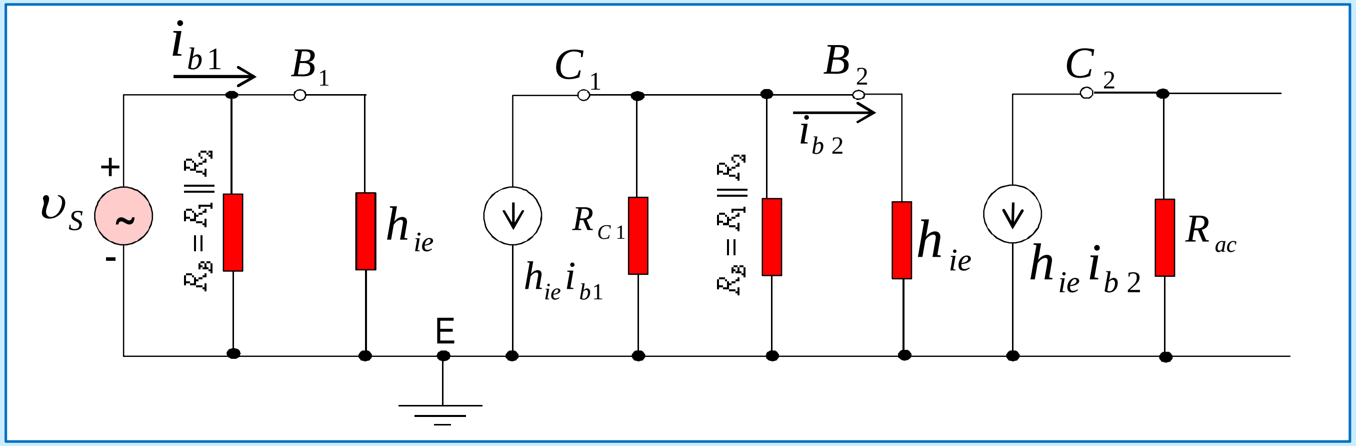


$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$A_1 = -\frac{h_{fe} R_{ac1}}{h_{ie}}$$

$$A_2 = -\frac{h_{fe} R_{ac2}}{h_{ie}}$$

$$A_{\upsilon m} = A_1 \times A_2$$

$$R_{ac2} = R_{C2} \parallel R_L = \frac{R_{C2} R_L}{R_{C2} + R_L}$$

A_1 is always less than A_2, because of lower R_{ac1} due to loading effect

Problem

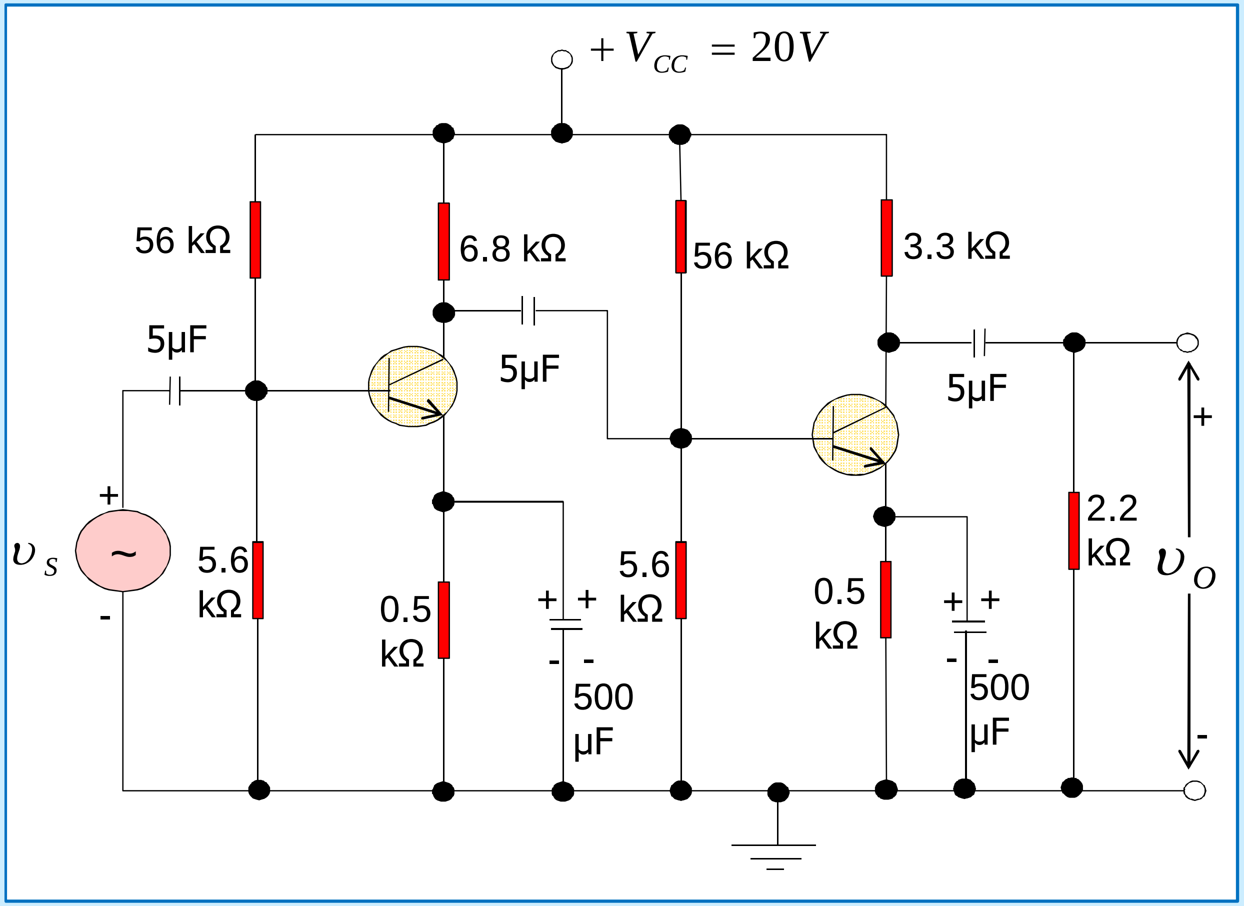
Calculate

- input impedance
- output impedance
- voltage gain

  both transistor

h_{fe} = 120

h_{ie} =1.1k ohm



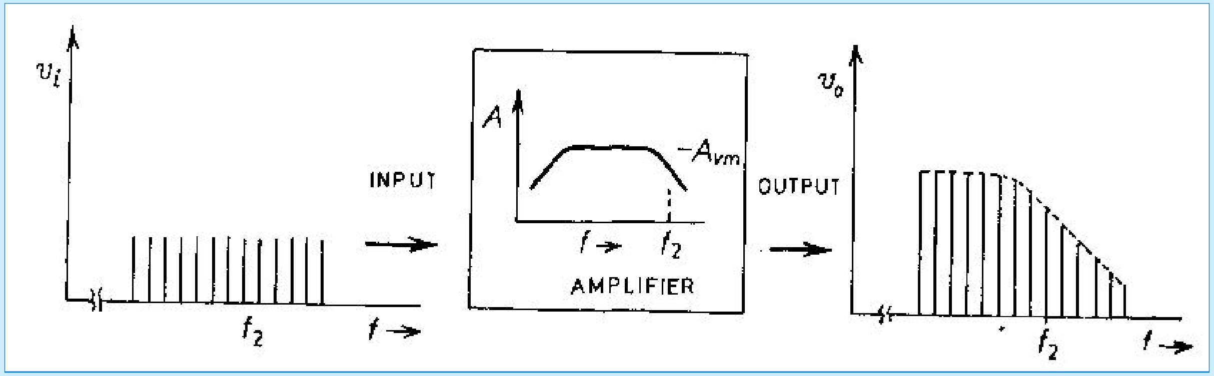
Distortion in Amplifiers

When wave shape of the output is not an exact replica of input wave

Caused by

- Reactive component and non-linear characteristic of transistor

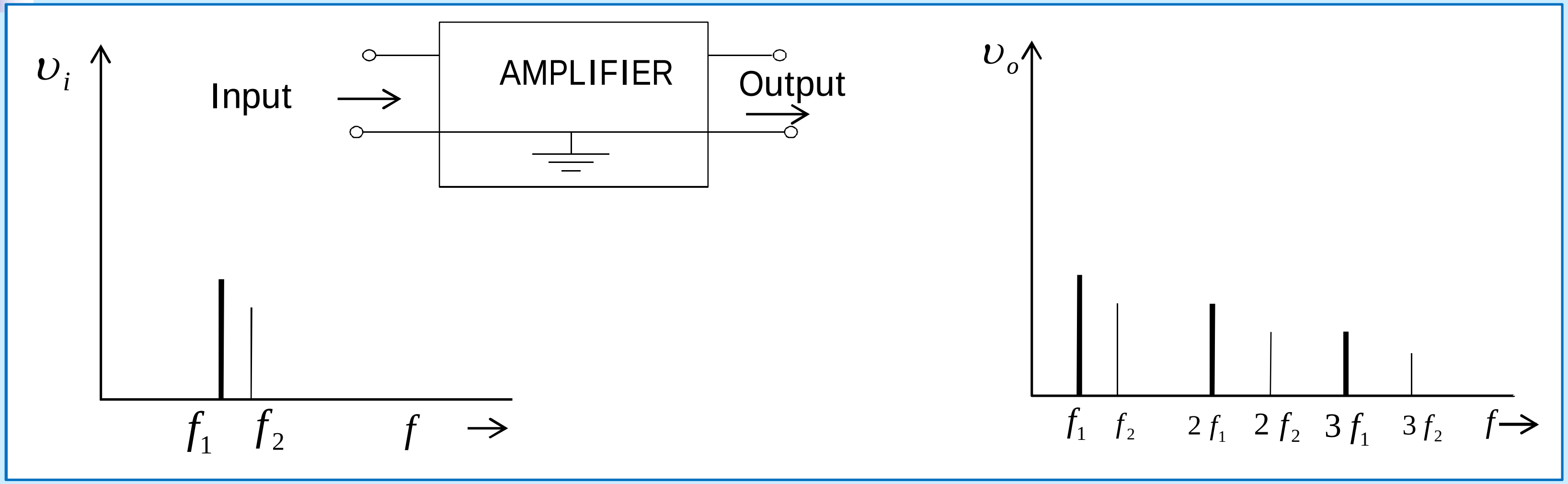
- Frequency distortion
  - Caused by electrode capacitance and other reactive components

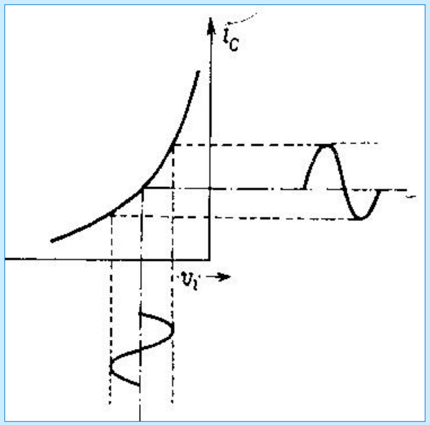


Contd.

- Phase distortion
  - Delay introduce by the amplifier is different for various frequency
  - Reactive components of the circuit are responsible for this distortion
- Harmonic distortion
  - Output contain new frequency components that are not present in the input. New frequency are harmonics of present in input
  - Happen due to non-linearity in the dynamic transfer characteristic curves

Contd.


υ_i
Input
AMPLIFIER
Output
υ_o
f_1 f_2 f
f_1 f_2 $2f_1$ $2f_2$ $3f_1$ $3f_2$ f


i_C
v_i

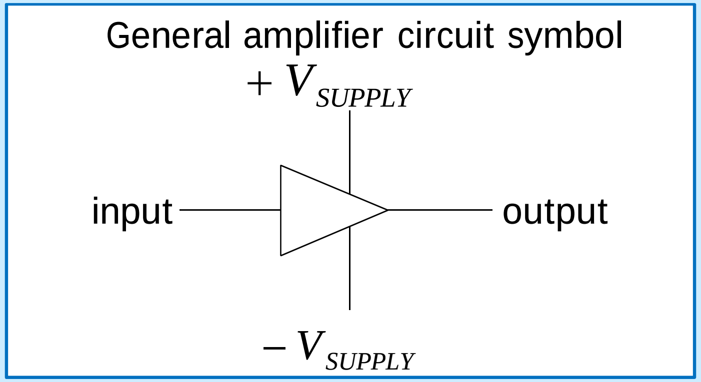
Operational-Amplifiers

Introduction

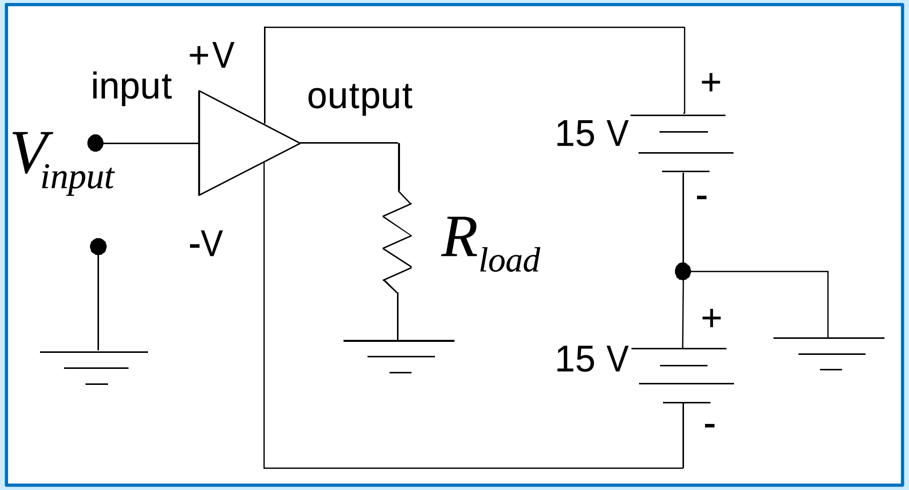
- The operational amplifier is most useful single device in analog electronic circuitry.
- With only few external components, it can perform a wide variety of analog signal processing tasks.
- One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly *negative* feedback, which constitutes the foundation of almost all automatic control processes.

Single-ended

- A "shorthand" symbol for an electronic amplifier is a triangle, the wide end signifying the input side and the narrow end signifying the output.

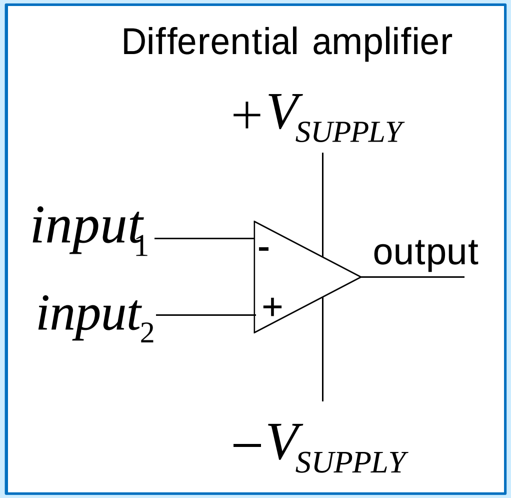


- To facilitate true AC output from an amplifier, we use a *split* or *dual* power supply, with two DC voltage sources connected in series with the middle point grounded, giving a positive voltage to ground (+V) and a negative voltage to ground (-V).



Differential amplifiers

- Most amplifiers have one input and one output. *Differential amplifiers* have two inputs and one output, the output signal being proportional to the difference in signals between the two inputs.
- The voltage output of a differential amplifier is determined by the following equation: $V_{out} = A_V(V_{noninv} - V_{inv})$



$(-)Input_1$	0	0	0	0	1	2.5	7	3	-3	-2
$(+)Input_2$	0	1	2.5	7	0	0	0	3	3	-7
$Output$	0	4	10	28	-4	-10	-28	0	24	-20

Voltage output equation = $V_{out} = A_V(Input_2 - Input_1)$

OR

$$V_{out} = A_V(Input_{(+)} - Input_{(-)})$$

The "operational" amplifier

- High-gain differential amplifiers came to be known as *operational amplifiers*, or *op-amps*, because of their application in analog computers' mathematical *operations*.
- *Op-amp* have extremely high voltage gain (A_V = 200,000 or more).
- Long before computers were built to electronically perform calculations by employing voltages and currents to represent numerical quantities.

$$i_c = C\frac{dv}{dt}$$

Where,

i_c = Instantaneous current through capacitor

C = Capacitance in farads

$\frac{dv}{dt}$ = Rate of change of voltage over time

$$F = m\frac{dv}{dt}$$

Where,

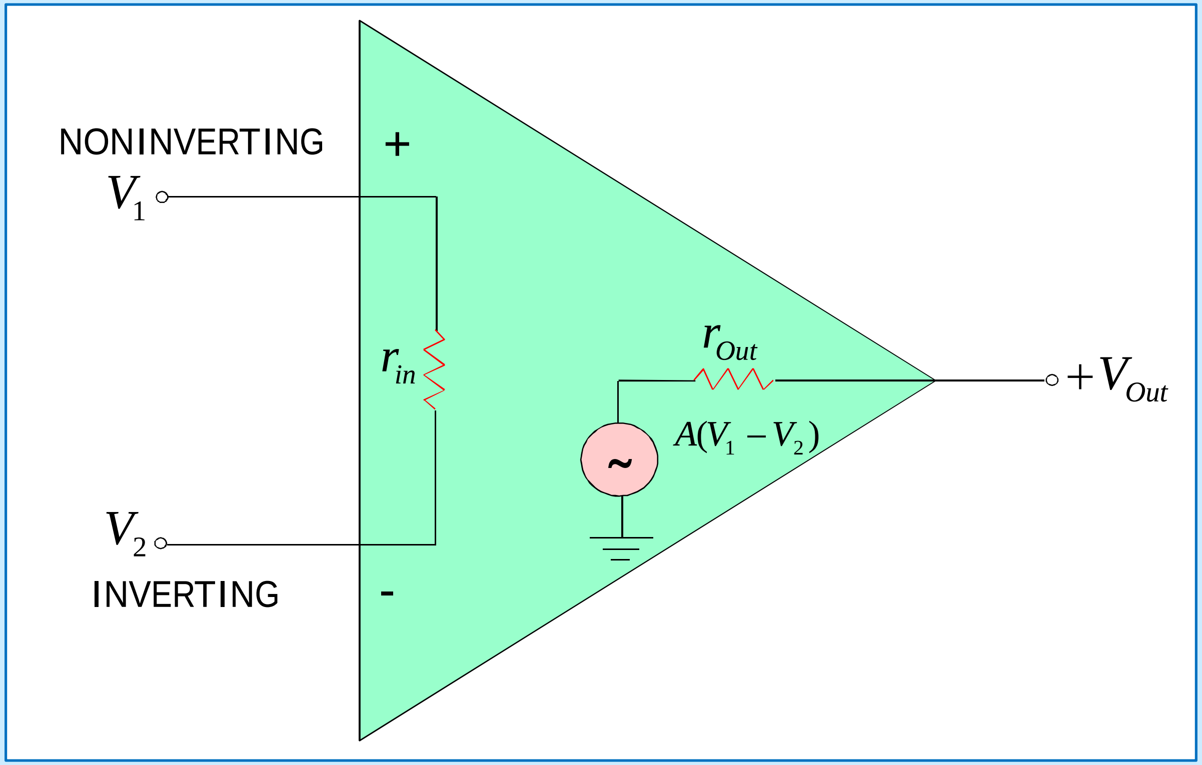
F = Force applied to object

m = Mass of object

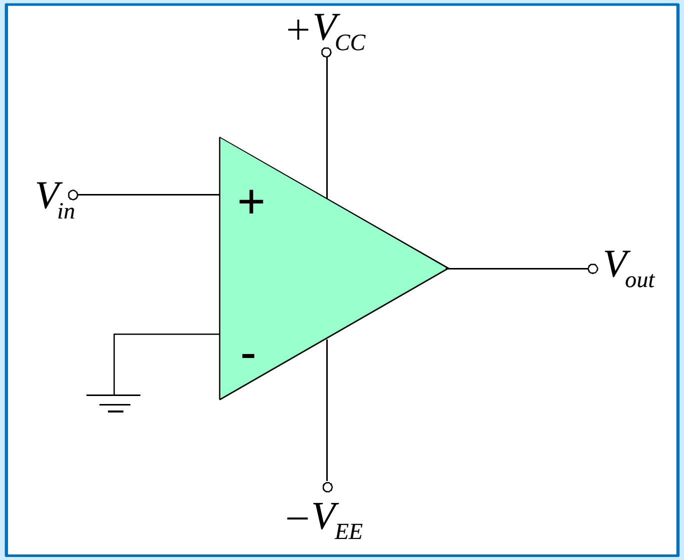
$\frac{dv}{dt}$ = Rate of change of velocity over time

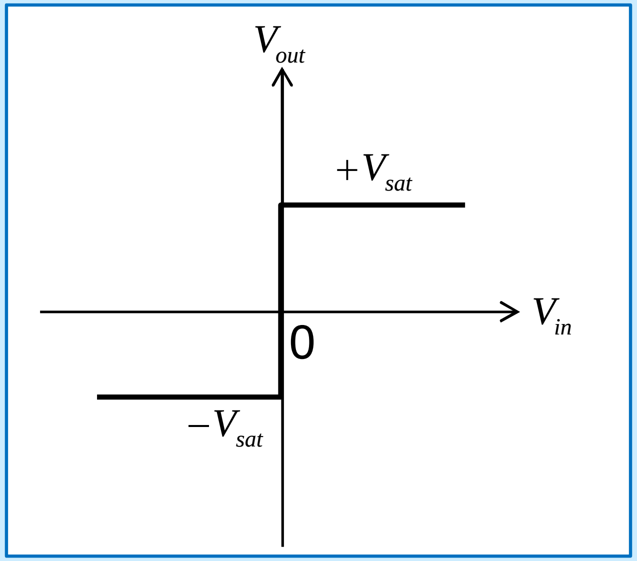
- Op-amps typically have very high input impedances and fairly low output impedances.

Op-amp electrical model

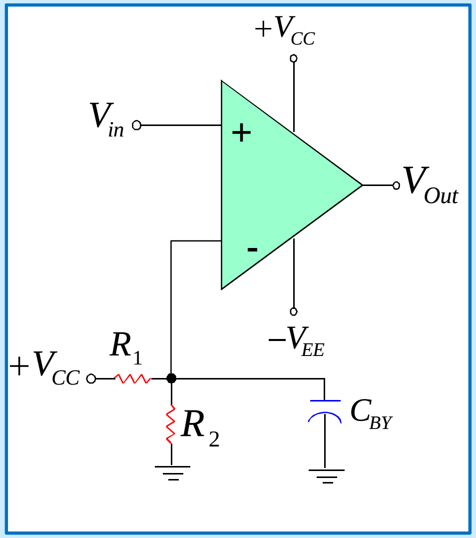


Comparator

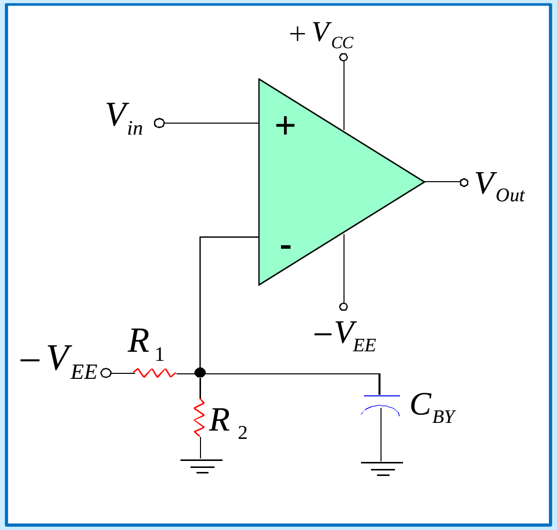


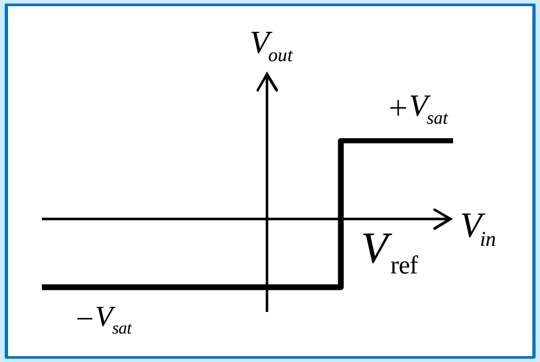


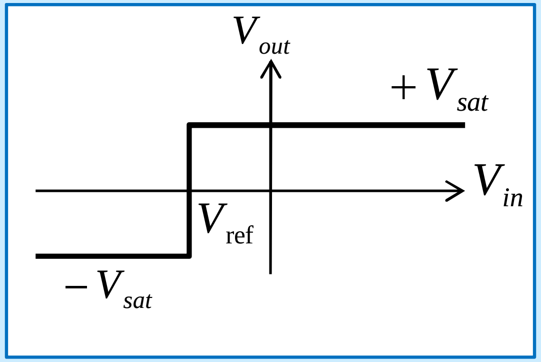
Moving trip point



$$\upsilon_{\text{ref}} = \frac{R_2}{R_1 + R_2} V_{CC}$$





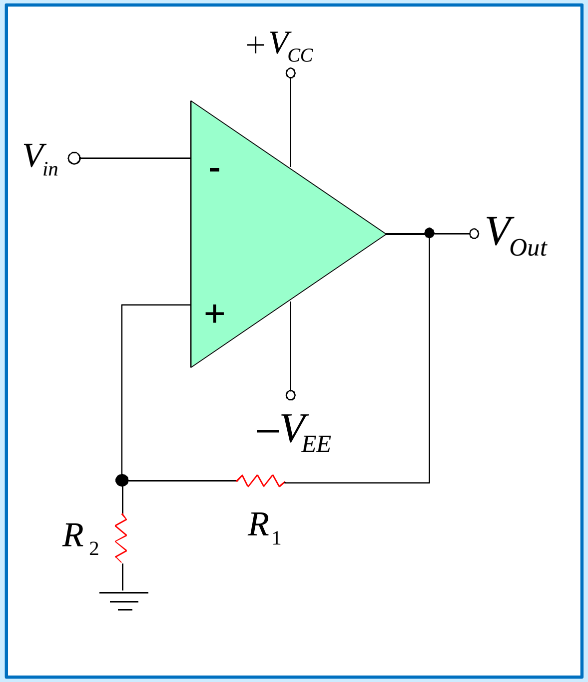


Schmitt Trigger

- Comparator contain noise, output may be erratic when input voltage is near to trip point
  - Noise causes output to jump back and forth between low and high states

Noise triggering can be avoided by schmitt trigger

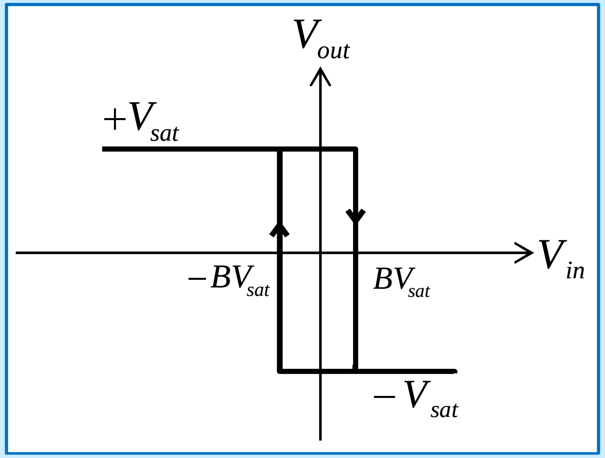
Contd.



$$B = \frac{R_2}{R_1 + R_2}$$

$$\upsilon_{\text{ref}} = +BV_{sat}$$

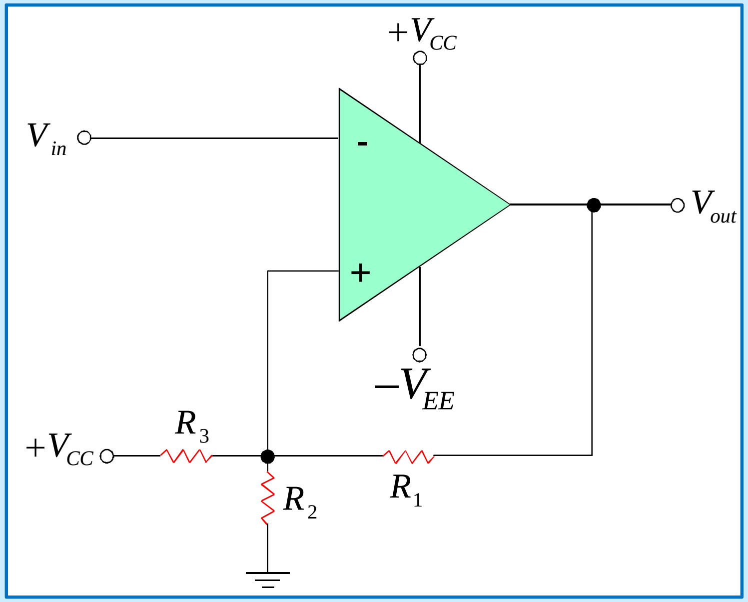
$$\upsilon_{\text{ref}} = -BV_{sat}$$

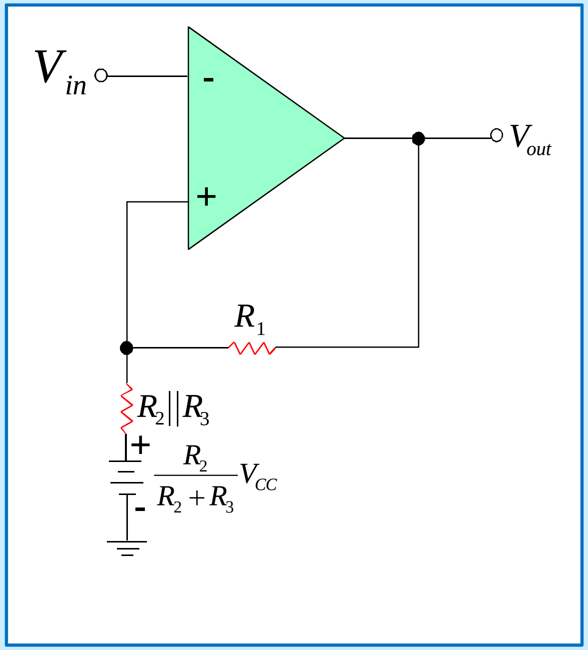


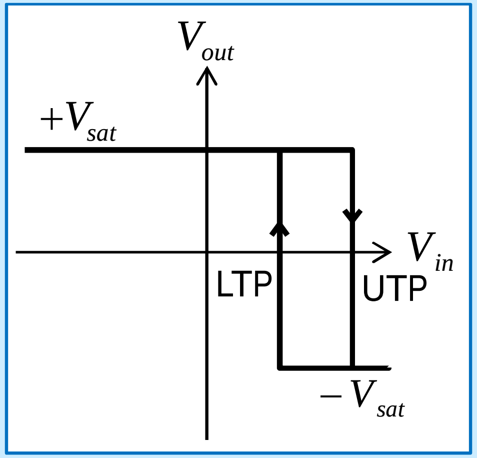
$$UTP = +BV_{sat}, \ and \ LTP = -BV_{sat}$$

Difference between UTP and LTP is called hysteresis, required to prevent false triggering due to noise

Moving trip point of schmitt trigger







$$\upsilon_{cen} = \frac{R_2}{R_2 + R_3} V_{CC}$$

$$B = \frac{R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3}$$

$$UTP = \upsilon_{cen} + BV_{sat}$$

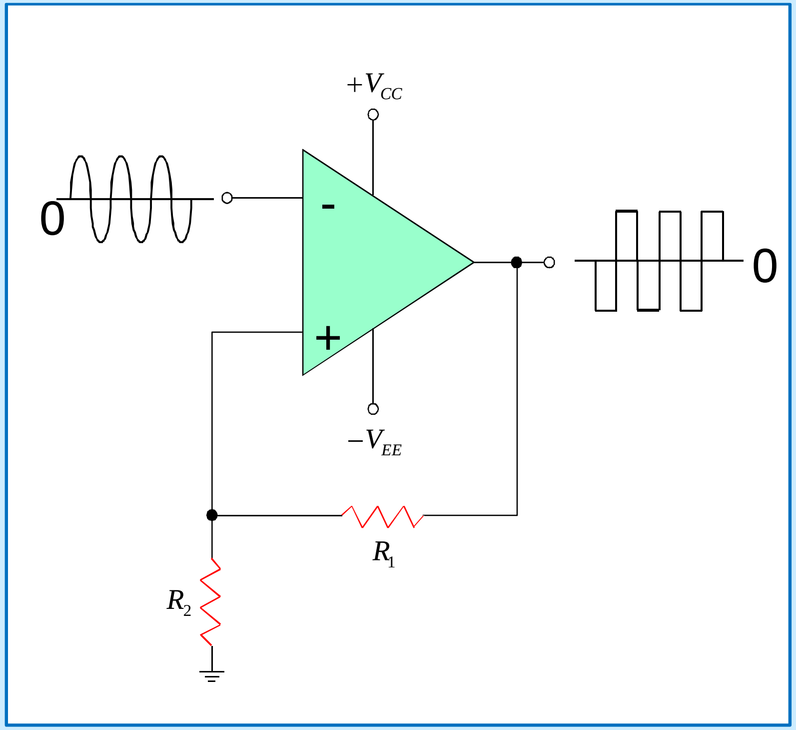
$$LTP = \upsilon_{cen} - BV_{sat}$$

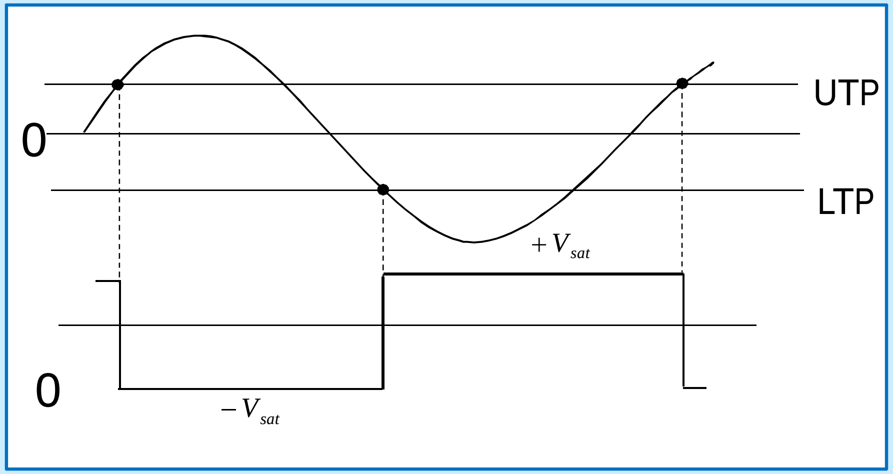
Problem

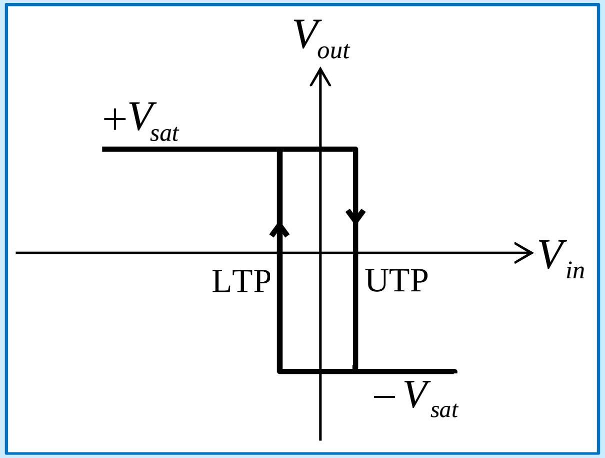
- Find UTP and LTP
  - Given

Vcc= 12 V, Vee=-12V, R2=R3=2 k ohm, R1= 100 k ohm

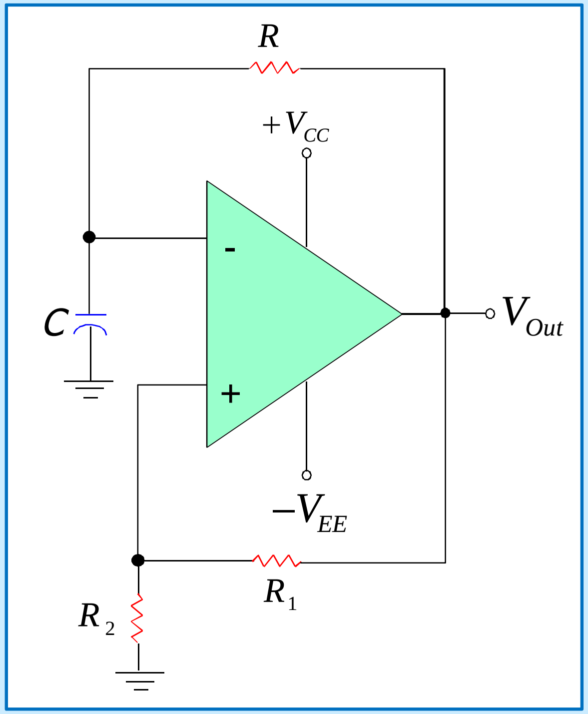
Sine to square waveform

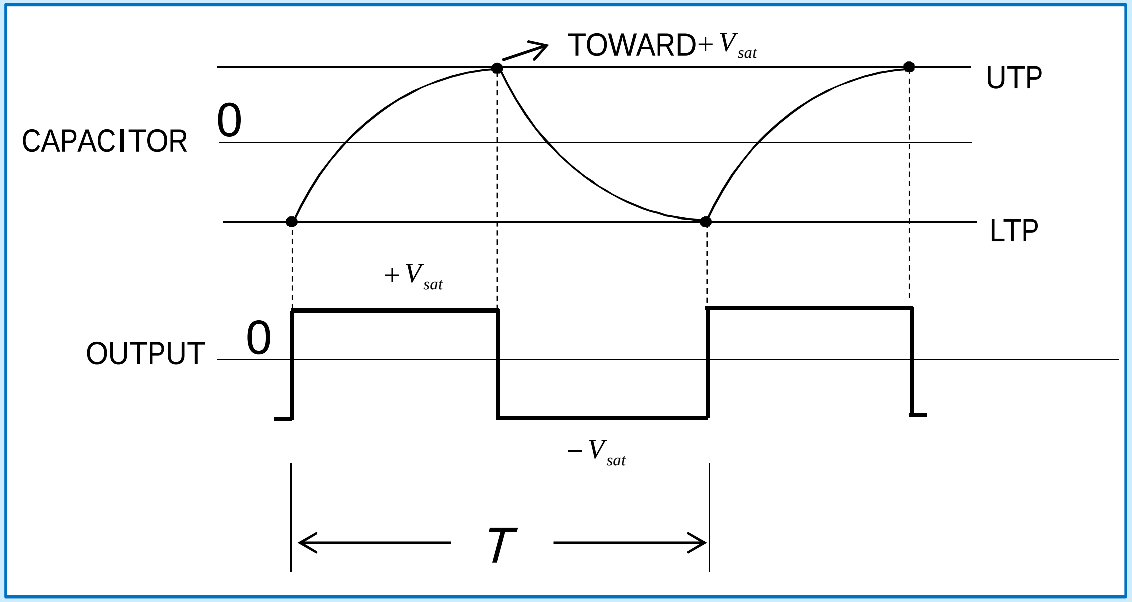






Relaxation oscillator

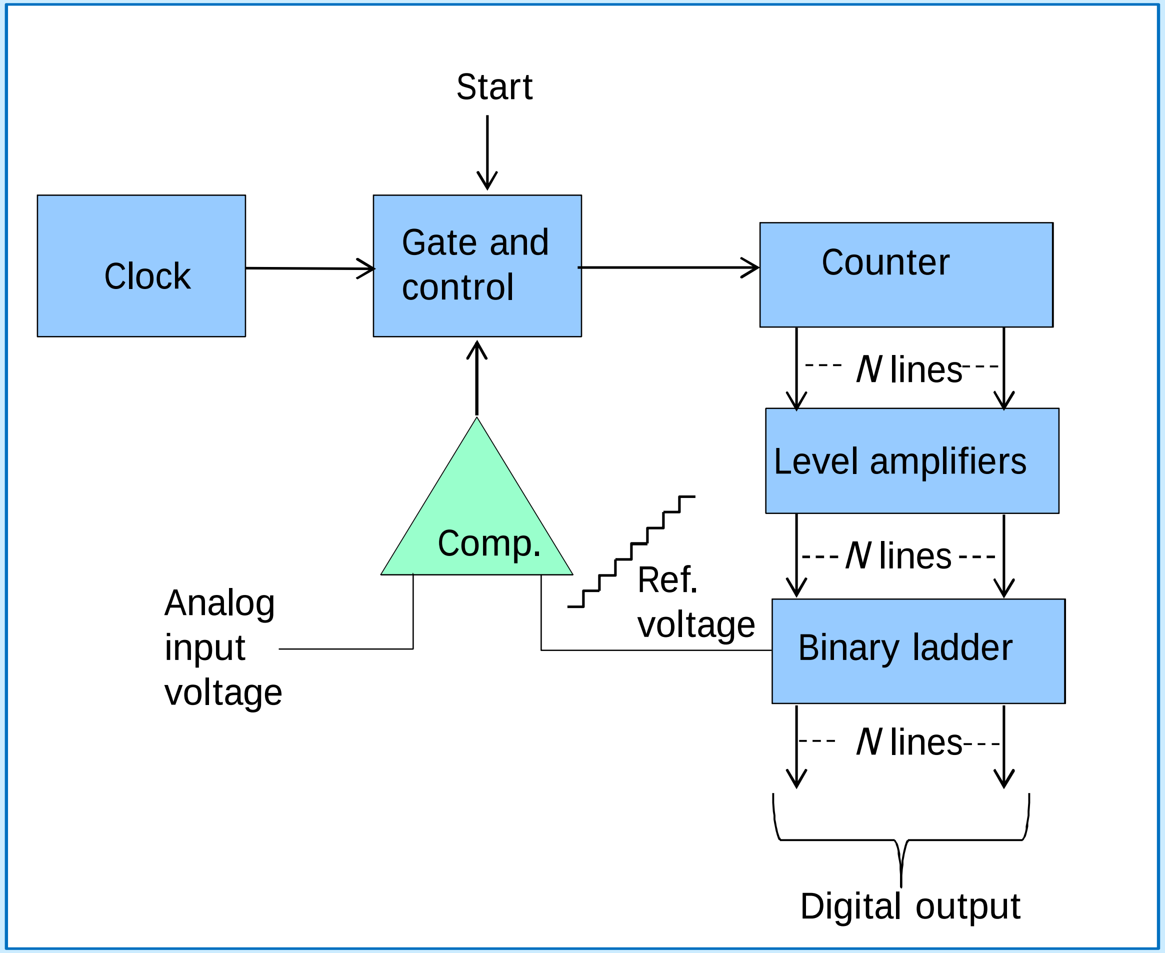




$$T = 2RC\ \ln \frac{1+B}{1-B}$$

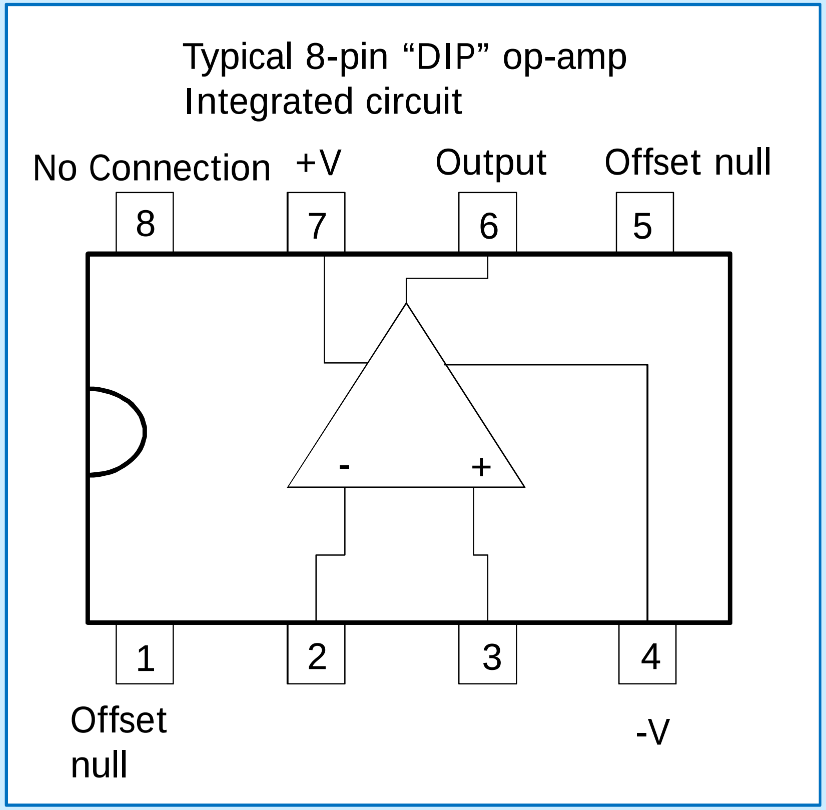
T = period of output signal
R = feedback resistance
C = capacitance
B = feedback fraction,

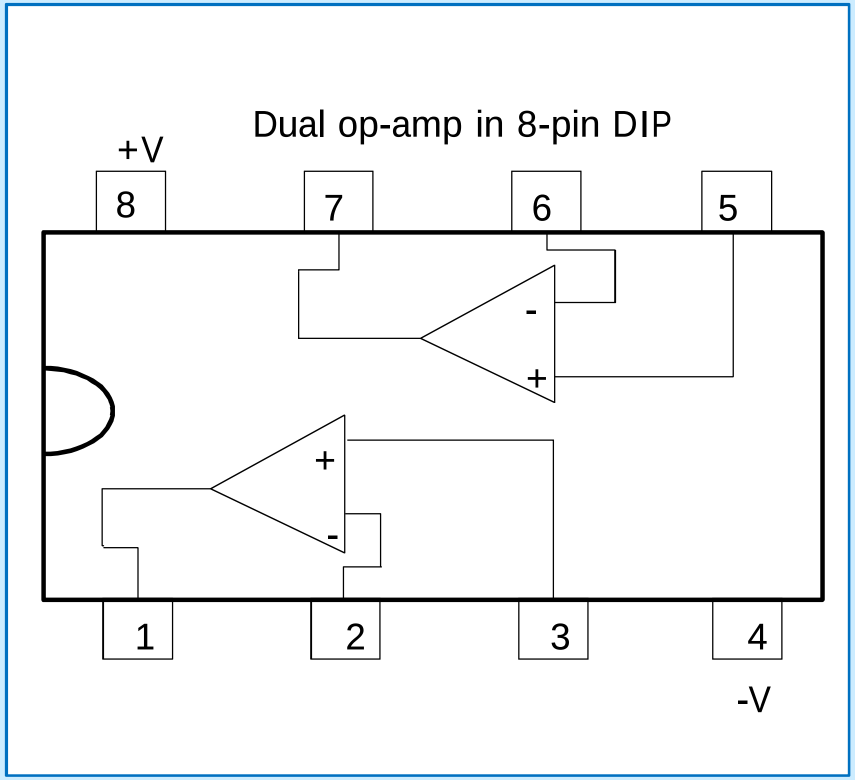
Counter based A/D convertor



OP-AMP IC's

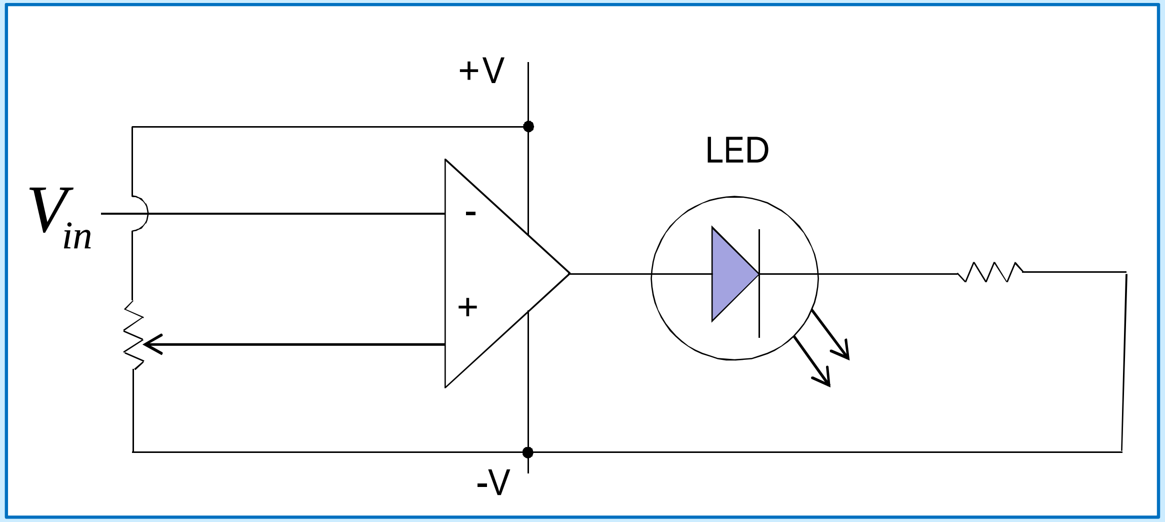
- Most popular 741





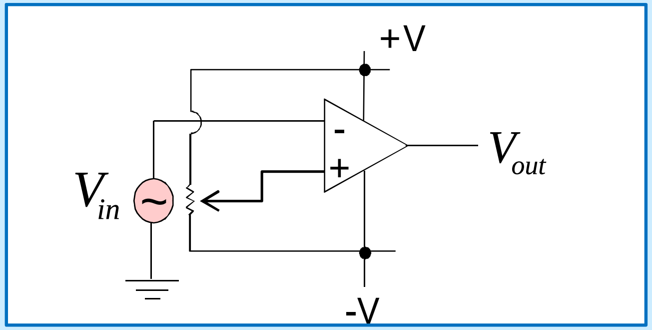
Comparator

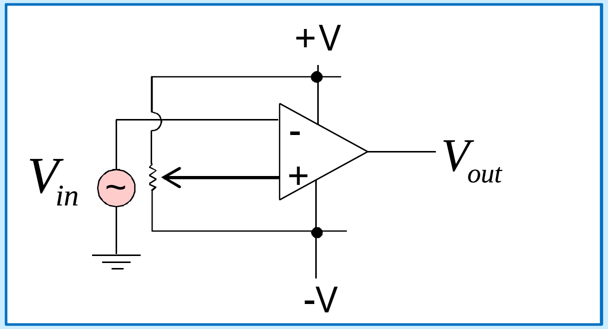
- To compare two voltages
  - Op-amps are used as signal *comparators*, operating in full cutoff or saturation mode depending on which input (inverting or non-inverting) has the greatest voltage.

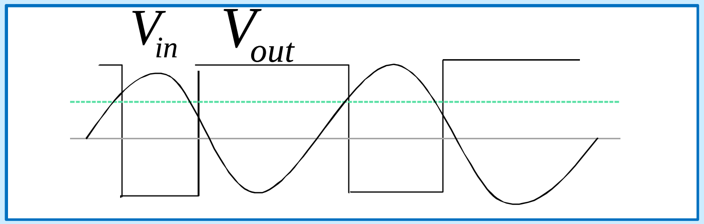


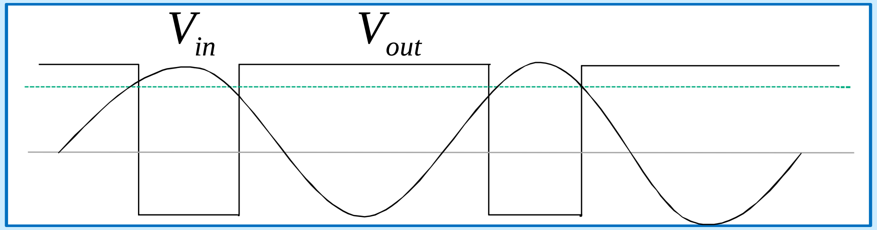
Pulse width modulation by comparator

One comparator application is *pulse-width modulator*, and is made by comparing a sine-wave AC signal against a DC reference voltage. As the DC reference voltage is adjusted, the square-wave output of the comparator changes its duty cycle (positive versus negative times). Thus, the DC reference voltage controls, or *modulates* the pulse width of the output voltage.

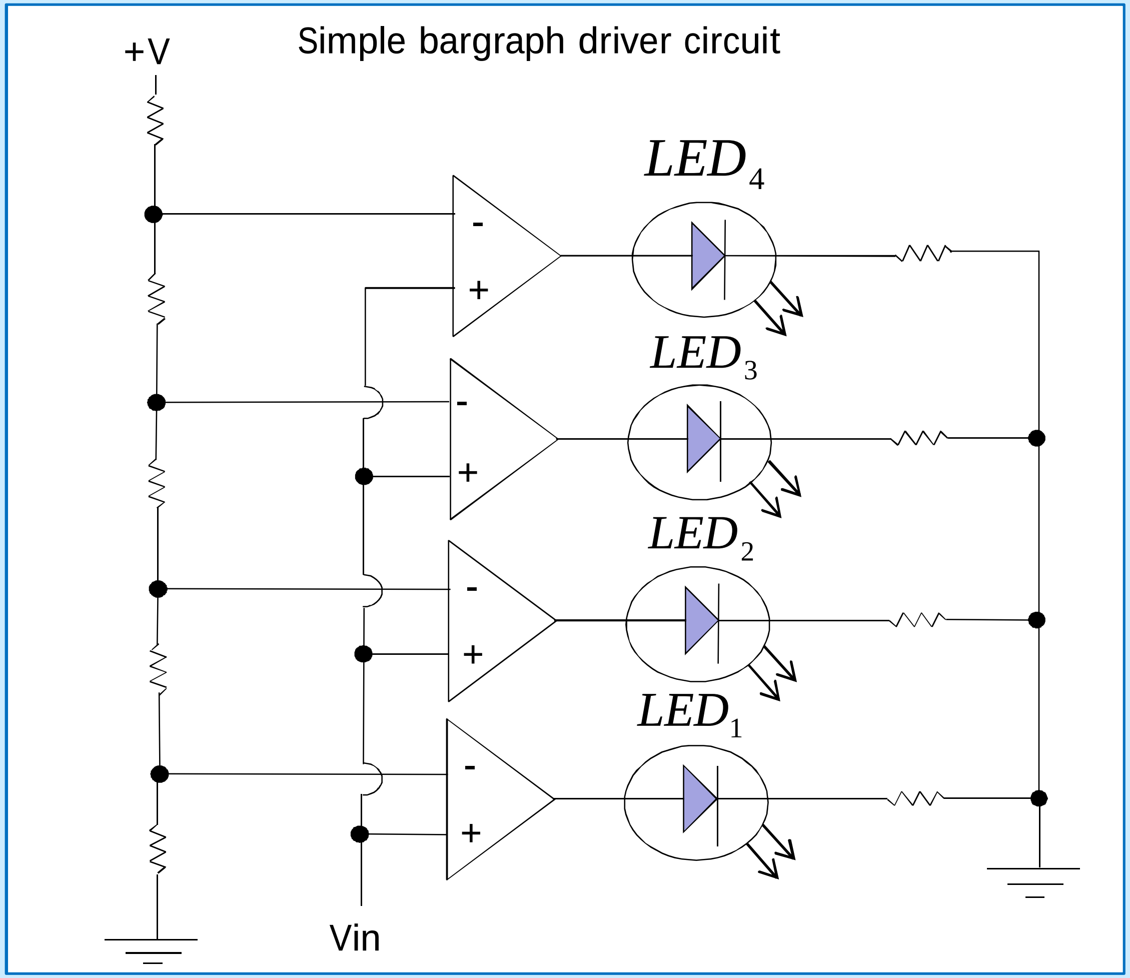




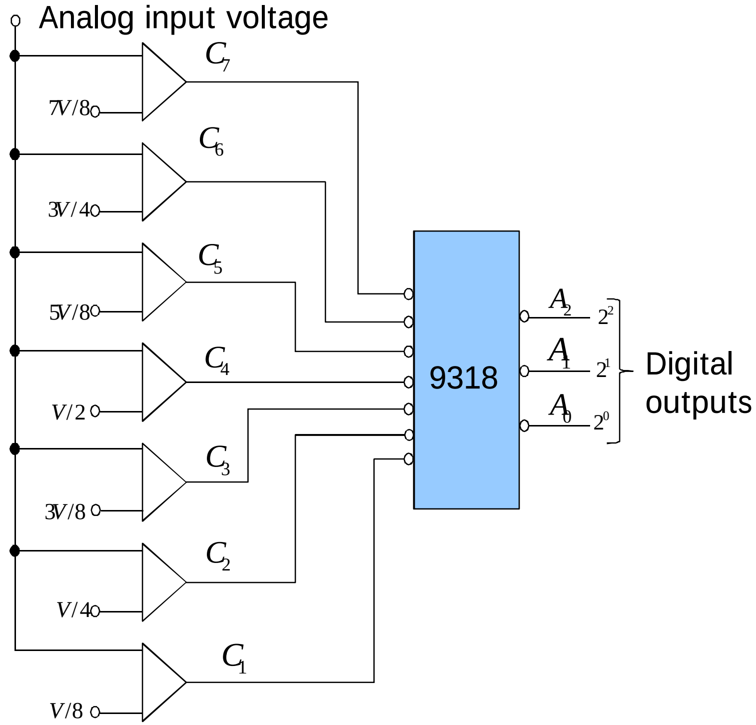




Analog to digital convertor



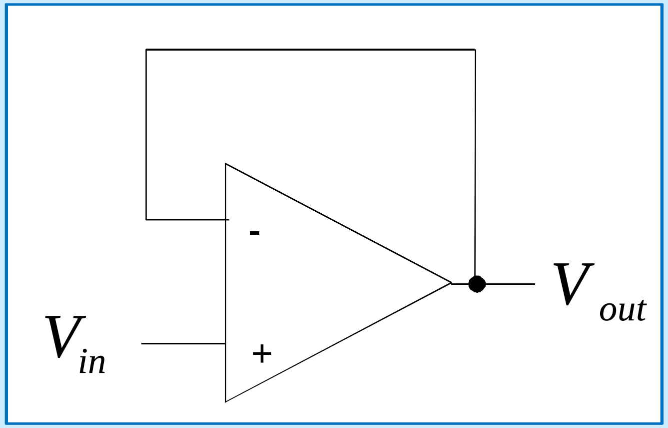
Analog to digital convertor



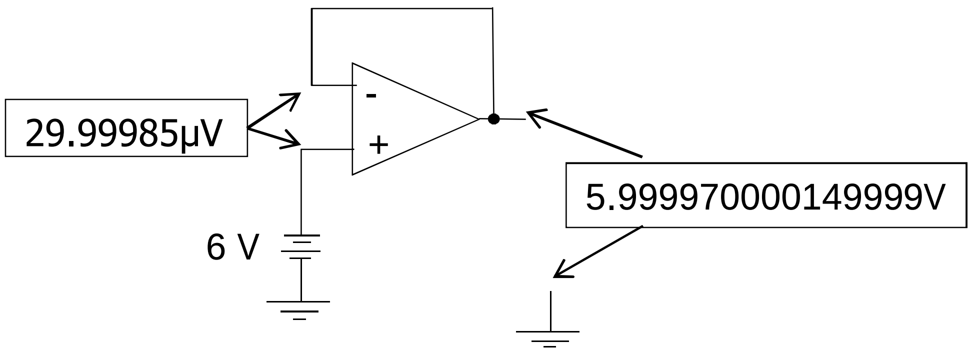
	Comparator for level							Binary output		
Input voltage	C_1	C_2	C_3	C_4	C_5	C_6	C_7	2^2	2^1	2^0
0 to $V/8$	Low	Low	Low	Low	Low	Low	Low	0	0	0
$V/8$ to $V/4$	High	Low	Low	Low	Low	Low	Low	0	0	1
$V/4$ to $3V/8$	High	High	Low	Low	Low	Low	Low	0	1	0
$3V/8$ to $V/2$	High	High	High	Low	Low	Low	Low	0	1	1
$V/2$ to $5V/8$	High	High	High	High	Low	Low	Low	1	0	0
$5V/8$ to $3V/4$	High	High	High	High	High	Low	Low	1	0	1
$3V/4$ to $7V/8$	High	High	High	High	High	High	Low	1	1	0
$7V/8$ to V	High	High	High	High	High	High	High	1	1	1

Negative feedback

- Connecting the output of an op-amp to its inverting (-) input is called *negative feedback*.
- When the output of an op-amp is *directly* connected to its inverting (-) input, a *voltage follower* will be created. Whatever signal voltage is impressed upon the noninverting (+) input will be seen on the output.
- An op-amp with negative feedback will try to drive its output voltage to whatever level necessary so that the differential voltage between the two inputs is practically zero. The higher the op-amp differential gain, the closer that differential voltage will be to zero.



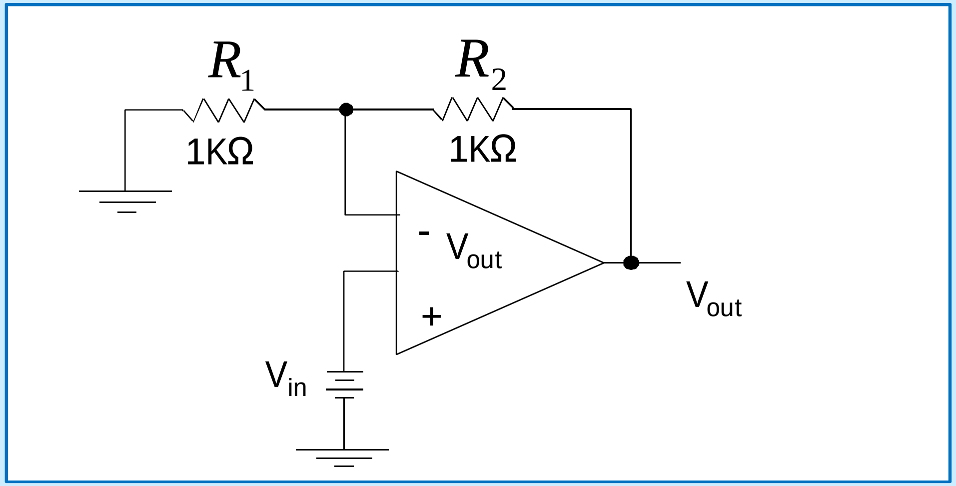
The effects of negative feedback



Divided feedback

Non-inverting Amplifier

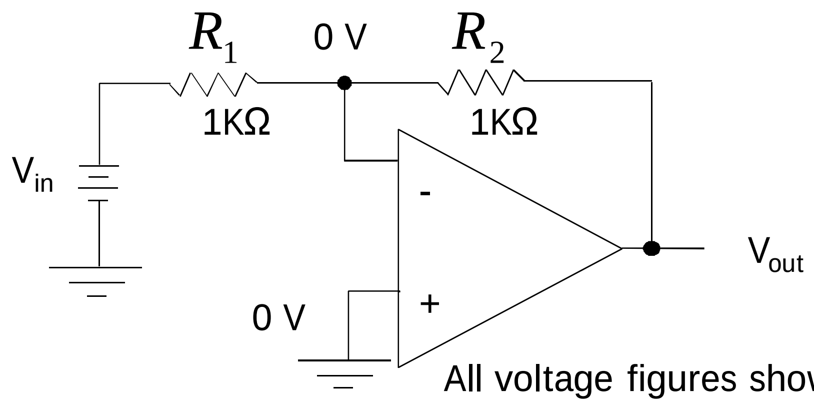
A negative-feedback op-amp circuit with the input signal going to the noninverting (+) input is called a *noninverting amplifier*. The output voltage will be the same polarity as the input. Voltage gain is given by the following equation: $A_V = (R_2/R_1) + 1$



Contd.

Inverting Amplifier

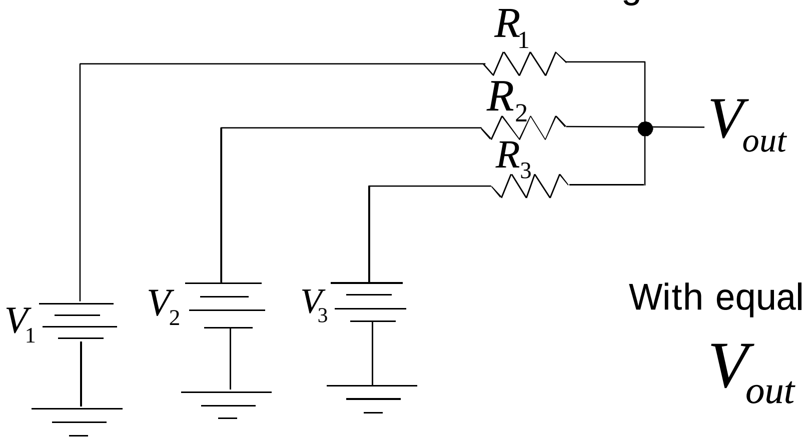
A negative-feedback op-amp circuit with the input signal going to the "bottom" of the resistive voltage divider, with the noninverting (+) input grounded, is called an *inverting amplifier*. Its output voltage will be the opposite polarity of the input. Voltage gain is given by the following equation: $A_V = R_2/R_1$



All voltage figures shown in reference to ground

Average circuit

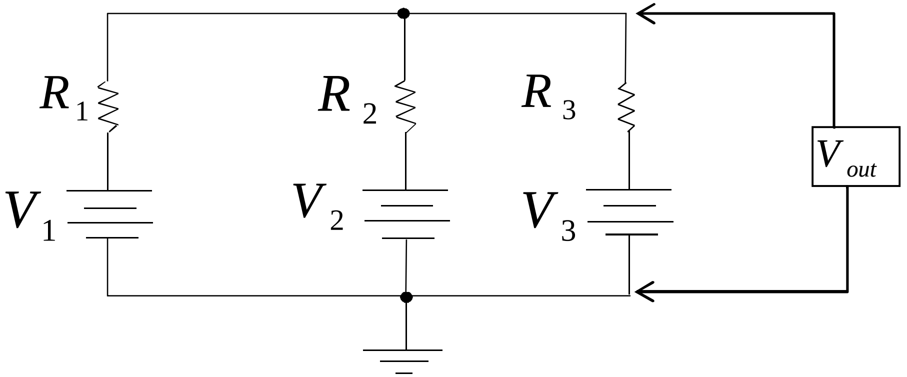
"Passive averager" Circuit



$$V_{out} = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

With equal value resistors:

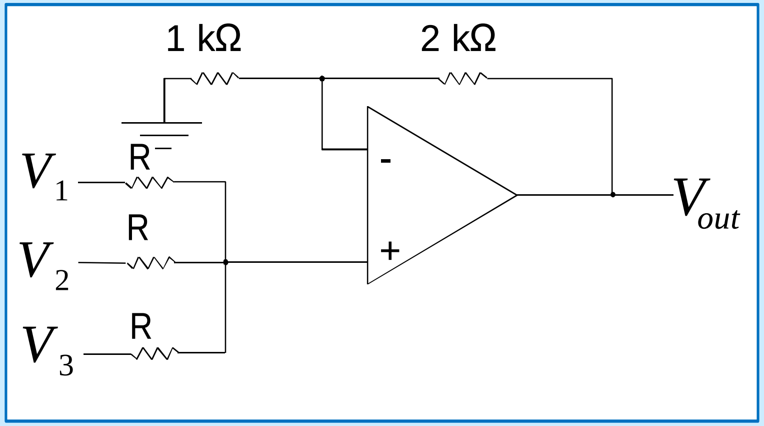
$$V_{out} = \frac{V_1 + V_2 + V_3}{3}$$



$$= \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

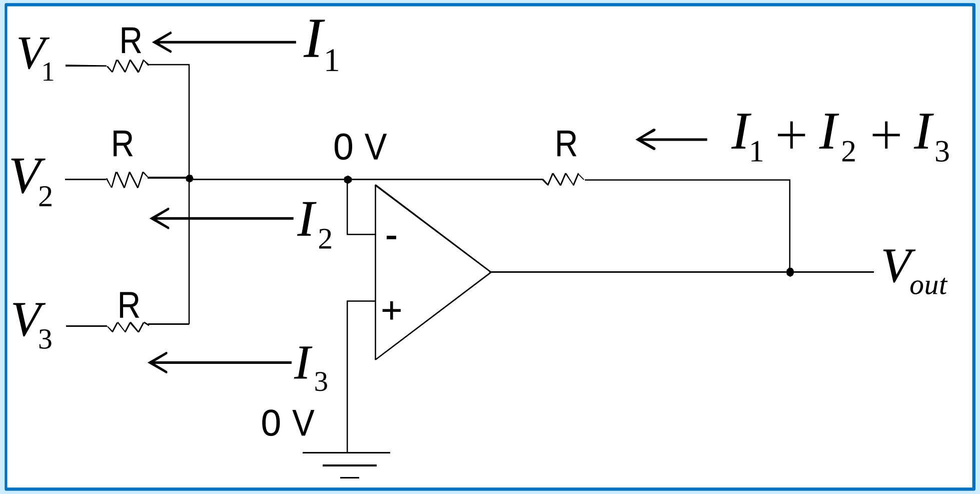
Summer circuit

- A summer circuit is one that sums, or adds, multiple analog voltage signals together. There are two basic varieties of op-amp summer circuits: noninverting and inverting.
- Summer circuits are quite useful in analog computer design.



$$V_{out} = 3\frac{V_1 + V_2 + V_3}{3}$$

$$V_{out} = V_1 + V_2 + V_3$$

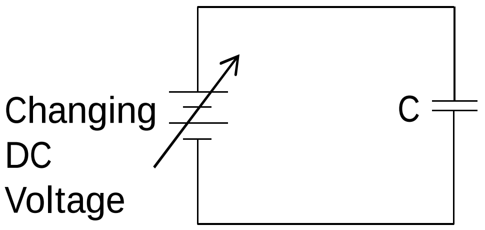


$$V_{out} = -(V_1 + V_2 + V_3)$$

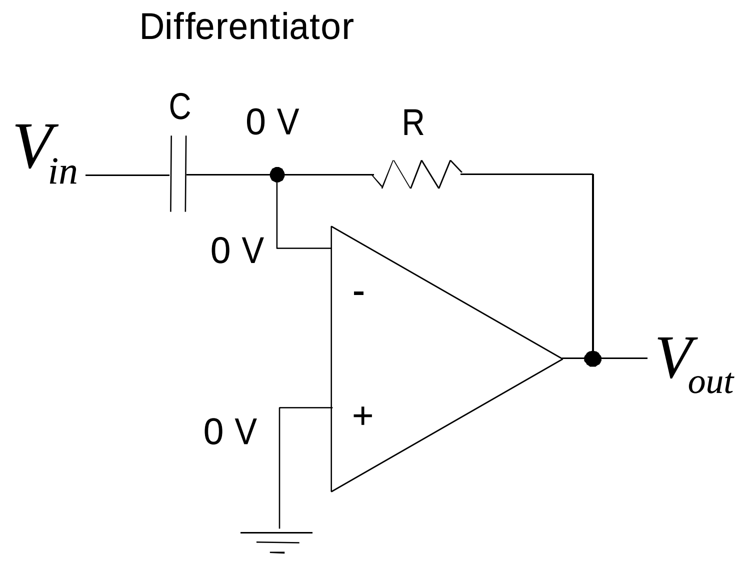
Differentiator circuits

Differentiator produces a voltage output proportional to the input voltage's rate of change.

Applications: analog computation, process control



$$i = C\frac{dv}{dt}$$

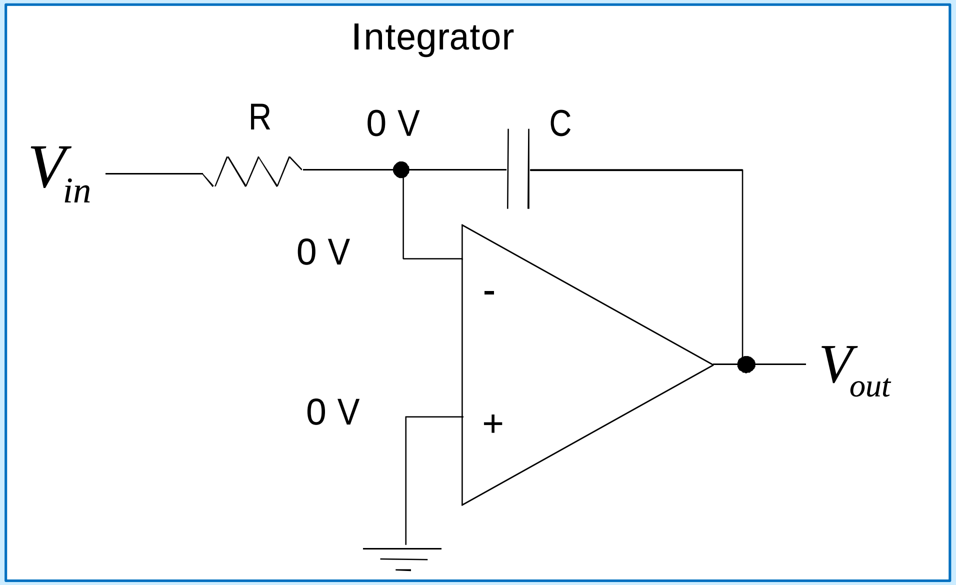


$$V_{out} = -RC\frac{dv_{in}}{dt}$$

Integrator circuits

integrator produces a voltage output proportional to the product (multiplication) of the input voltage and time

Applications: analog computation, process control



$$\frac{dv_{out}}{dt} = -\frac{V_{in}}{RC}$$

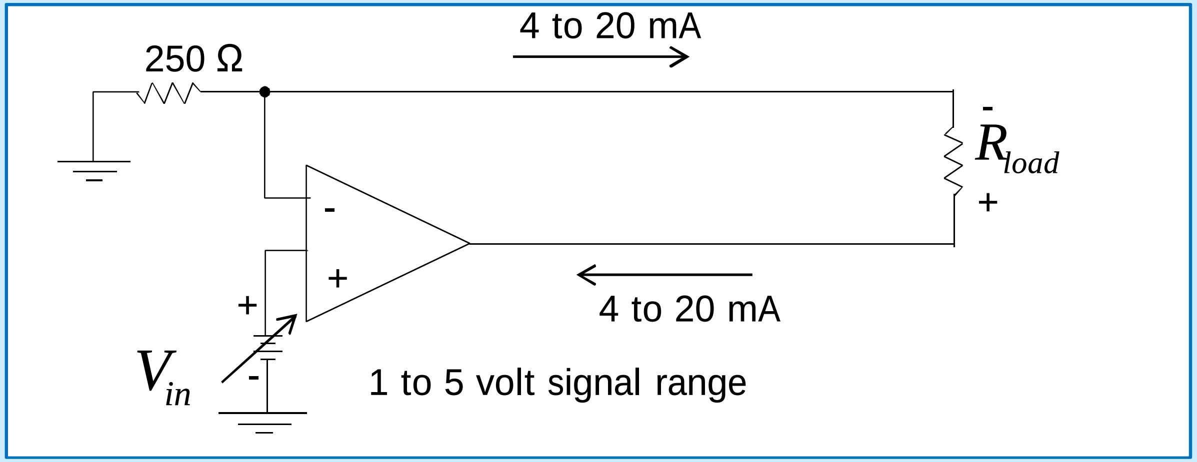
OR

$$V_{out} = \int_0^t -\frac{V_{in}}{RC} dt + c$$

Where,
C=Output voltage at start time (t=0)

Voltage-to-current signal conversion

- Voltage signals are relatively easy to produce directly from transducer devices, whereas accurate current signals are not.
- DC current signals are often used in preference to DC voltage signals as analog representations of physical quantities. Current in a series circuit is absolutely equal at all points in that circuit regardless of wiring resistance, whereas voltage in a parallel-connected circuit may vary from end to end because of wire resistance.



Current independent of load resistance

Slew rate

- Maximum rate of output voltage change

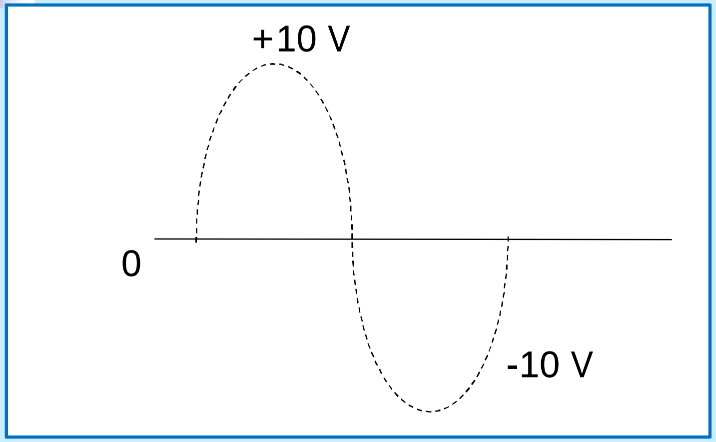
$$i = C\frac{dv}{dt}$$

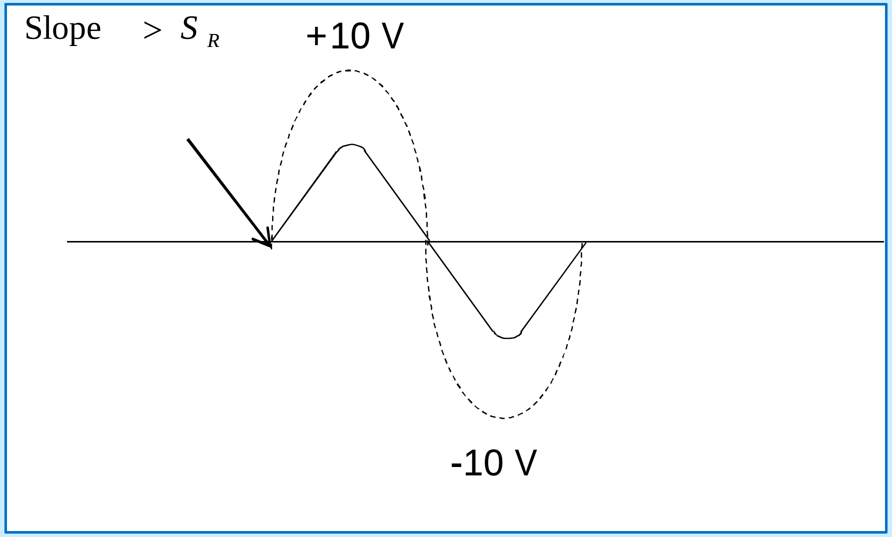
$$\frac{dv}{dt} = \frac{i}{C}$$

$$\frac{dv_{out}}{dt} = \frac{I_{\max}}{C_c}$$

$$\frac{dv_{out}}{dt} = \frac{60\,\mu A}{30\,pF} = 2\,V/\mu s$$

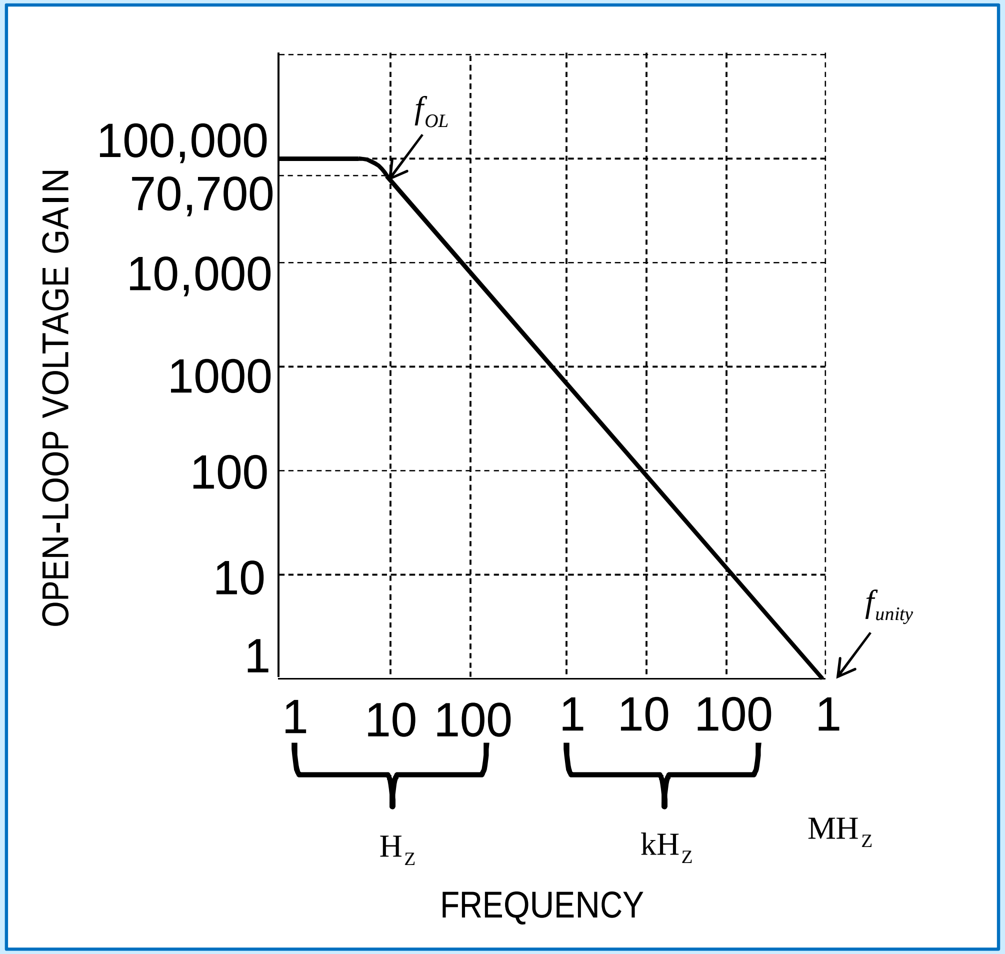
Slew rate distortion



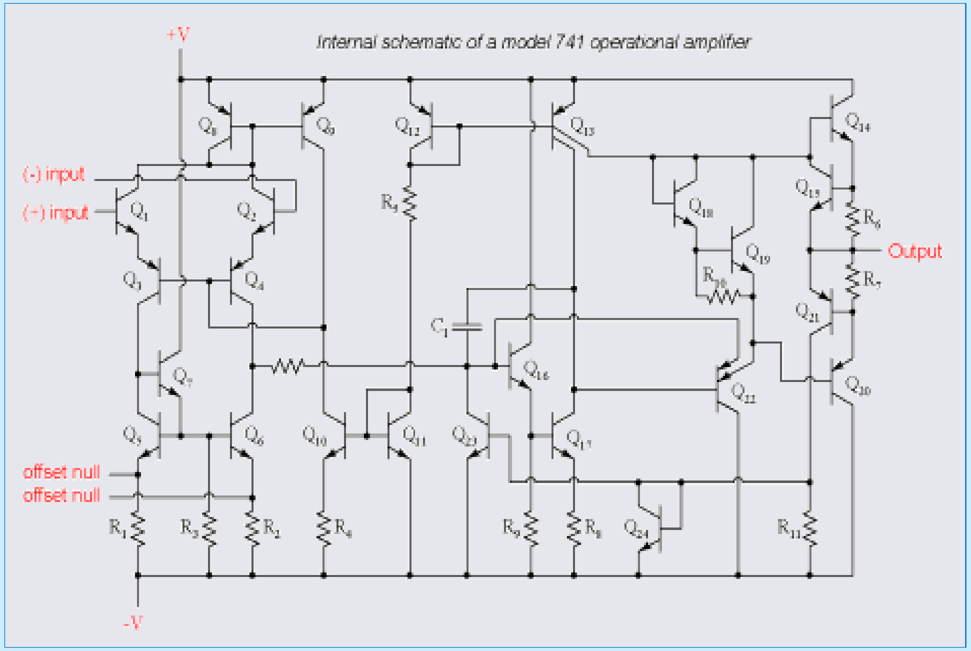


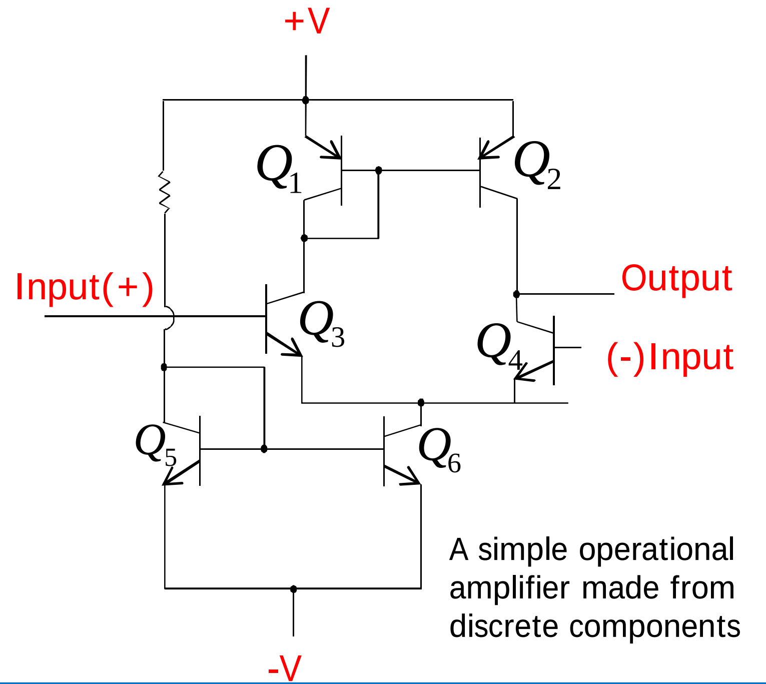
Frequency response of Op-amp

- Directly coupled amplifier
- Gain bandwidth product constant



Op-amp Models and circuits



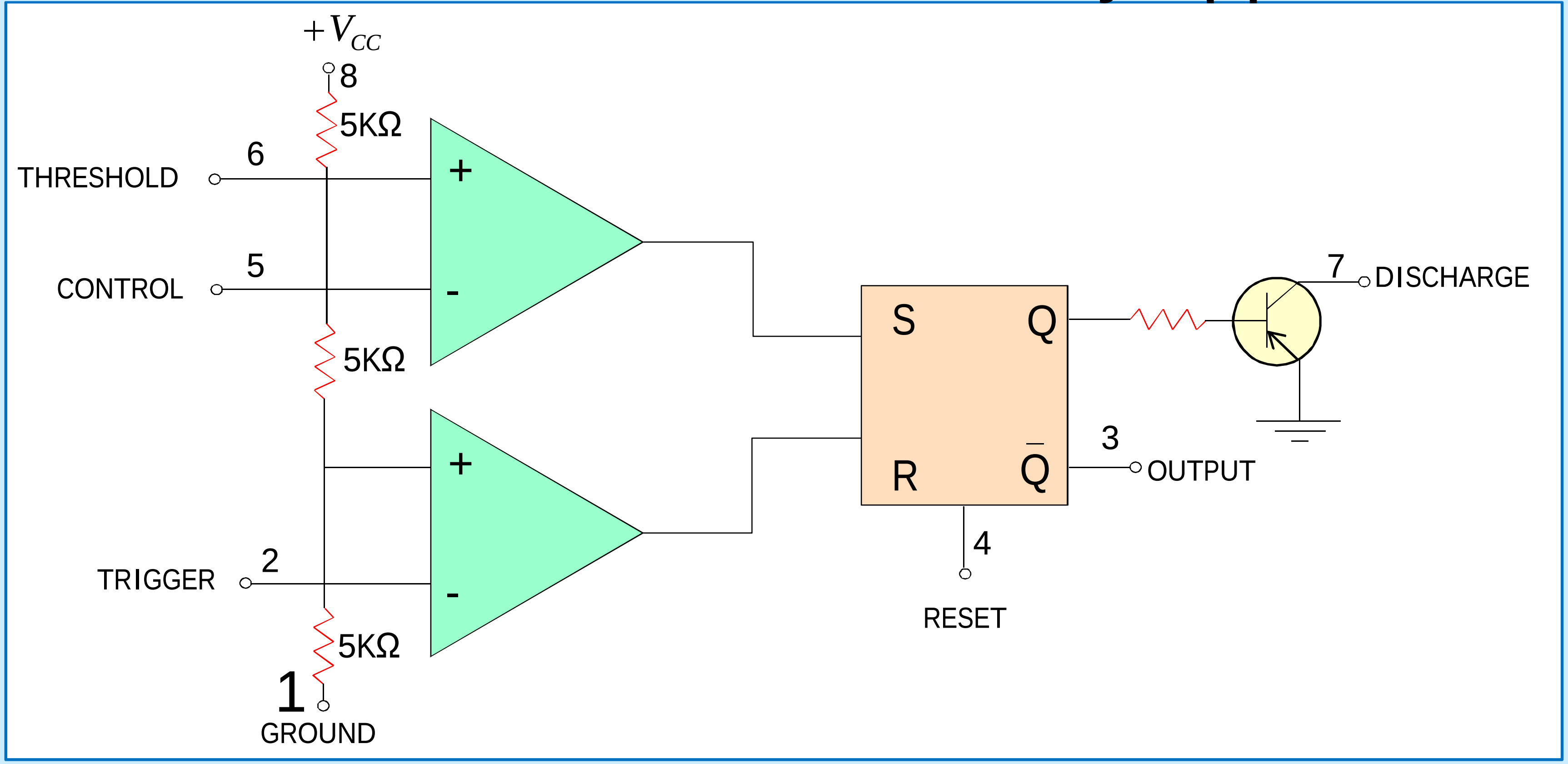


A simple operational amplifier made from discrete components

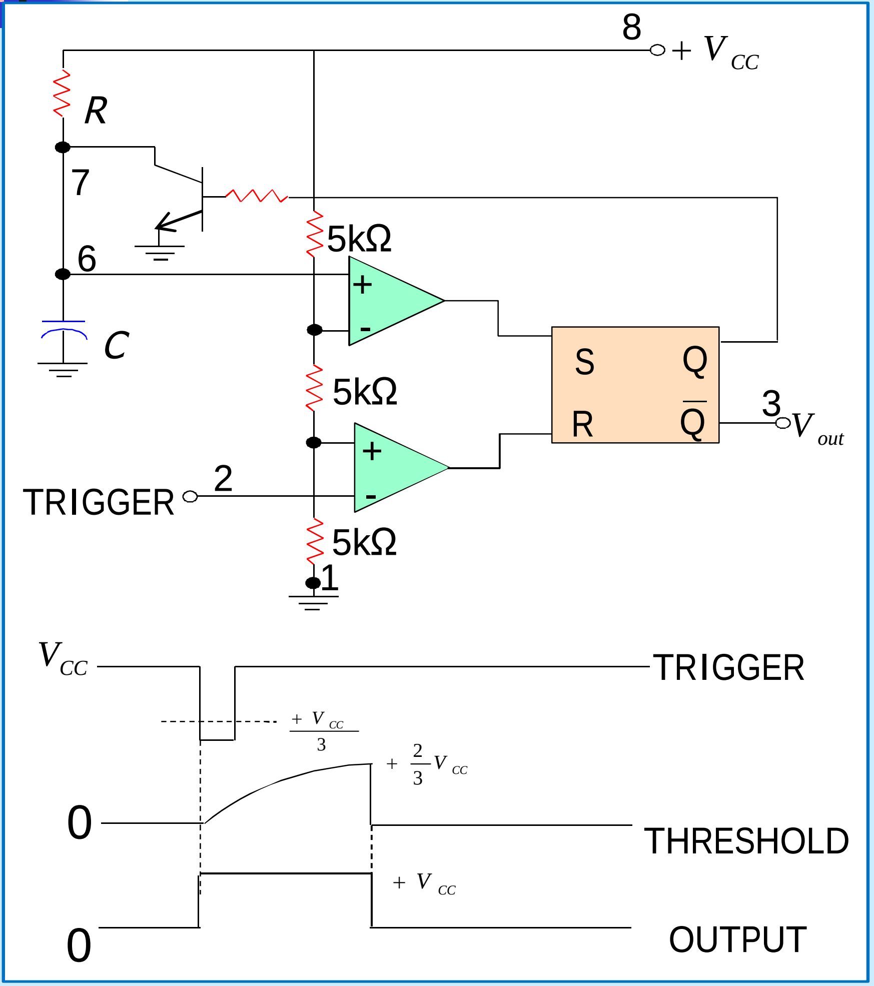
555 Timer

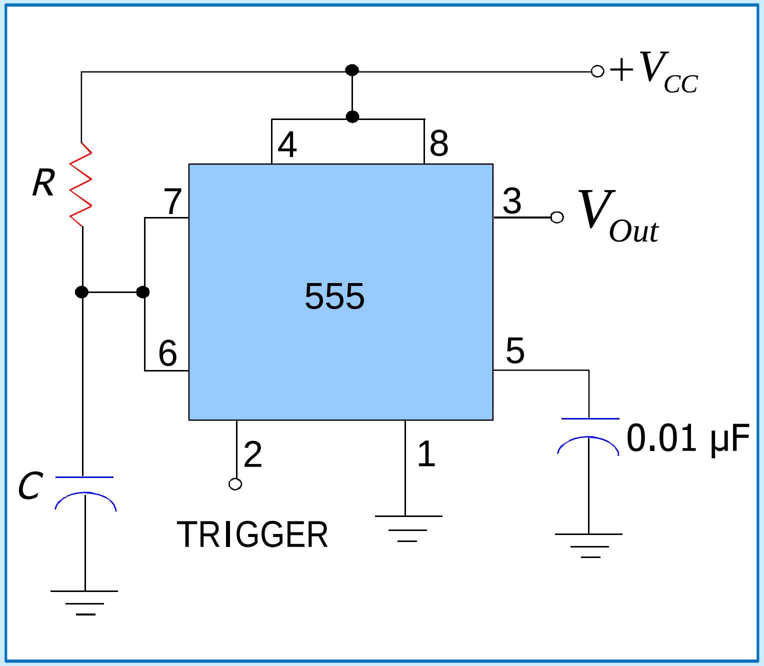
555 Timer

- Versatile IC, have so many application



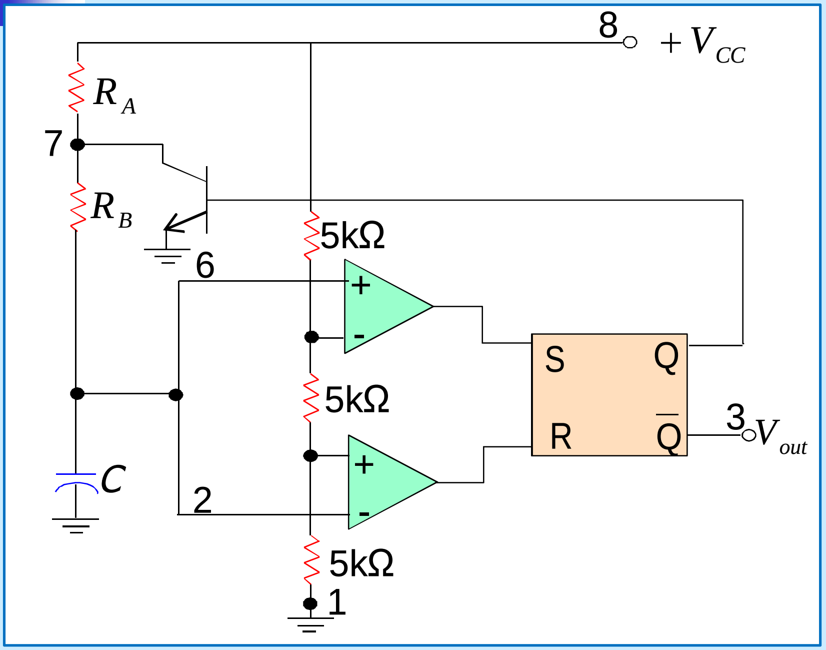
Monostable Operation

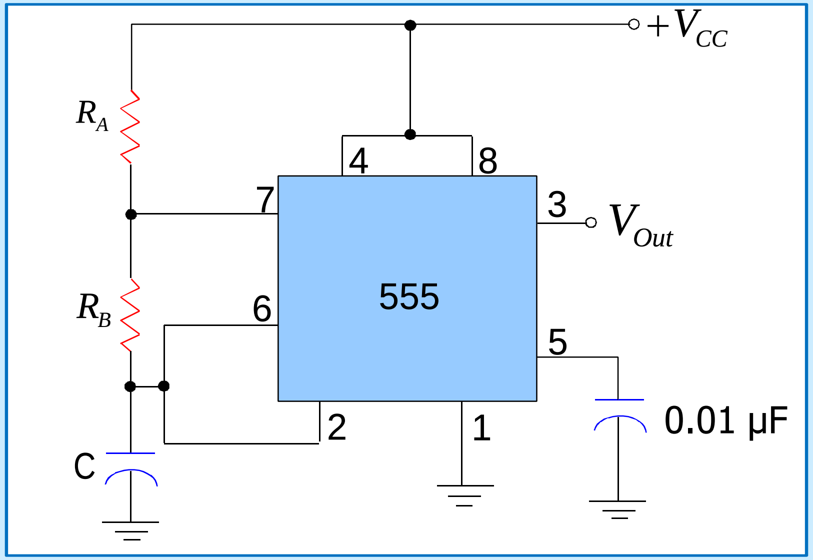




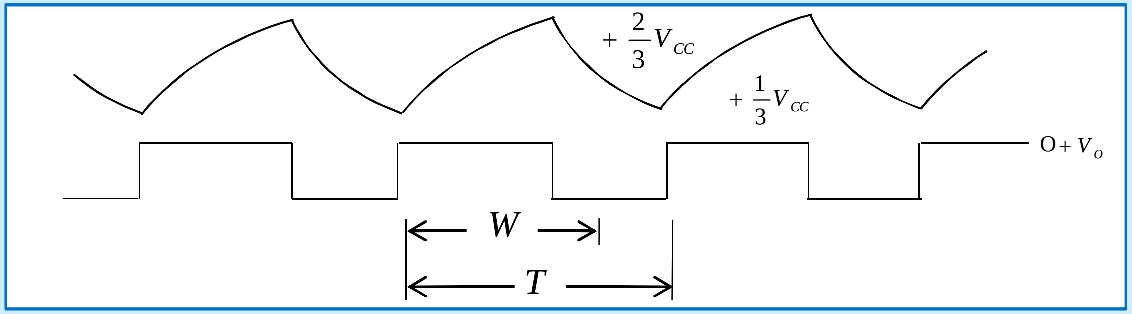
$$W = 1.1RC$$

Astable Operation





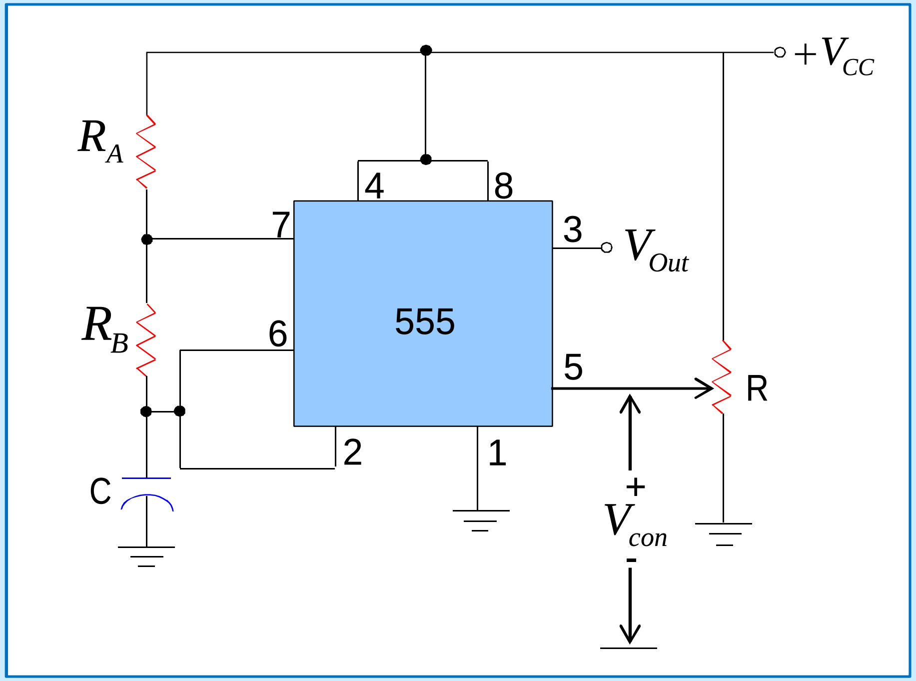
$$D = \frac{W}{T} \times 100\%$$

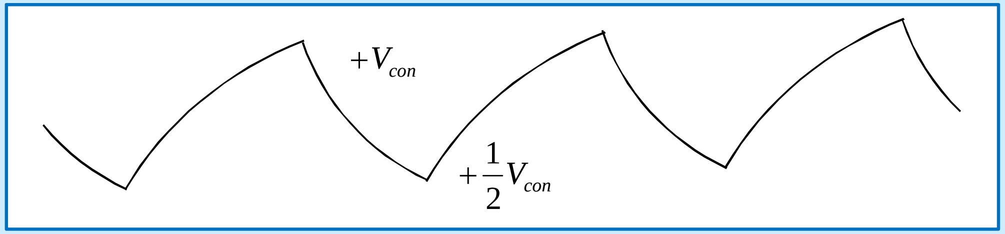


$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

Voltage control Oscillator





Active Filter

Active filters

Frequency selective switch that passes a specified band of frequency and blocks/attenuates signals of frequency outside

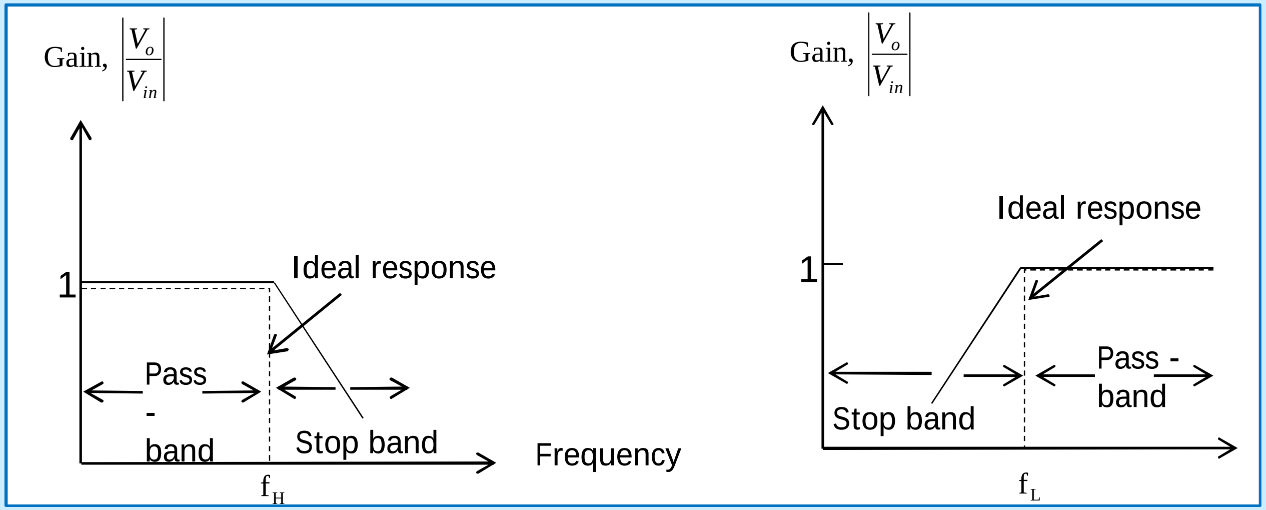
- Analog or digital
- Passive or active
- Audio (AF) or radio frequency (RF)

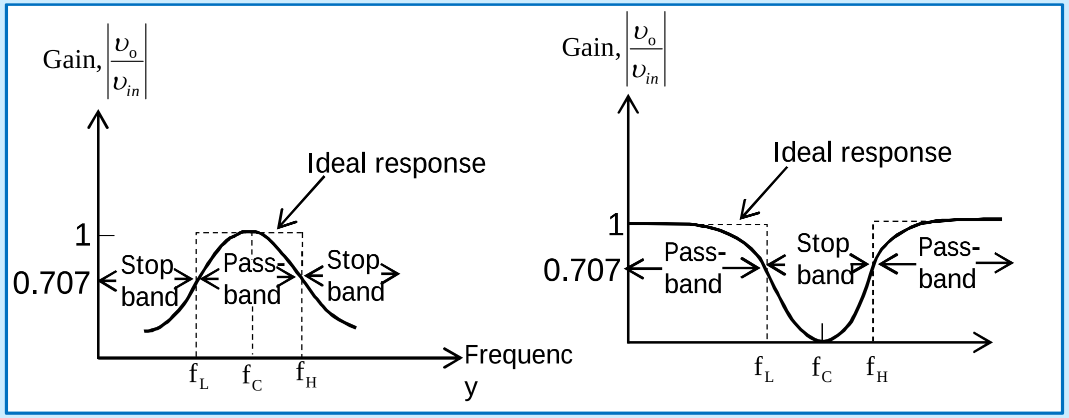
Analog Active-RC (audio) filter

- Active filter advantage
  - Gain frequency adjustment
  - No loading problem
  - Cost

Commonly used filters

- Low pass filter
- High pass filter
- Band pass filter
- Band reject filter

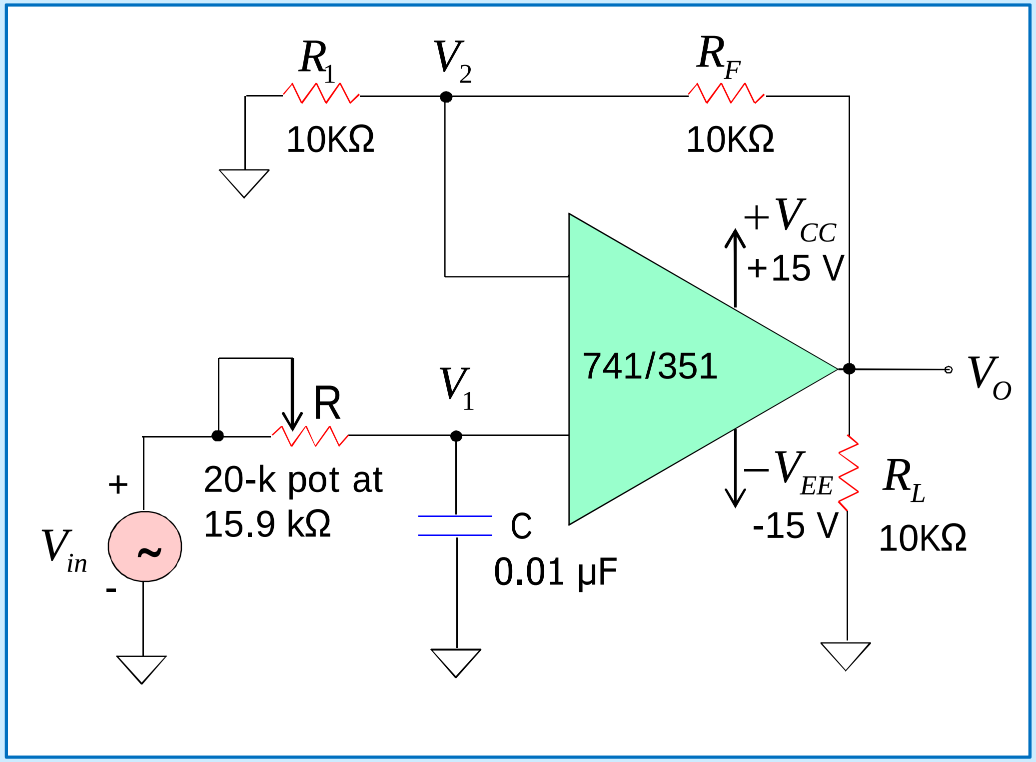




Classification of active filter

- Butterworth
  - Flat passband and flat stopband
- Chebyshev
  - Ripple passband and flat stopband
- Cauer
  - Ripple passband and ripple stopband

First order low pass butterworth filter



$$j = \sqrt{-1} \text{ and } -jX_C = \frac{1}{j2\pi fC}$$

$$V_1 = \frac{V_{in}}{1 + j2\pi fRC}$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{V_{in}}{1 + j2\pi fRC}$$

$$\upsilon_1 = \frac{-jX_C}{R - jX_C} \upsilon_{in}$$

$$\frac{\upsilon_o}{\upsilon_{in}} = \frac{A_F}{1 + j(f / f_H)}$$

Contd.

$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^2}}$$

$$A_F = 1 + \frac{R_F}{R_1} = \text{passband gain of the filter}$$

$$f = \text{frequency of the input signal}$$

$$f_H = \frac{1}{2\pi RC} = \text{high cutoff frequency of the filter}$$

1. At very low frequencies, that is, $f < f_H$,

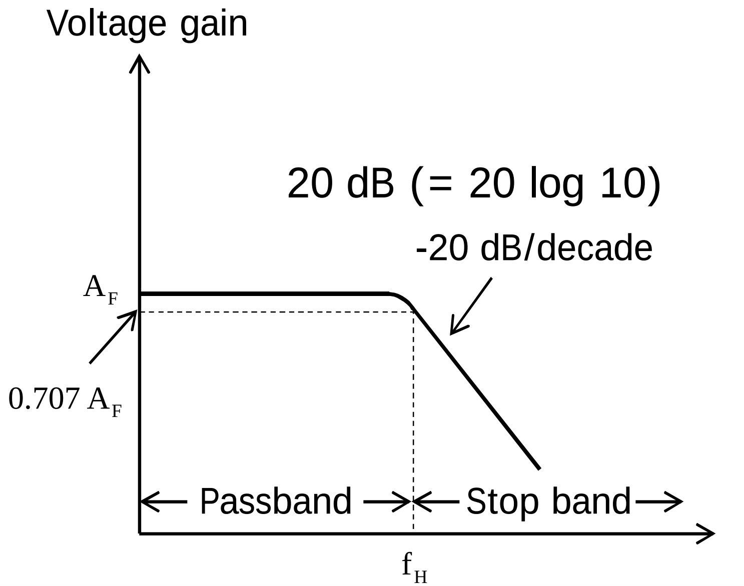
$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| \cong A_F$$

2. At 3 dB (= 20 log 0.707)

$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707 A_F$$

3. At $f > f_H$,

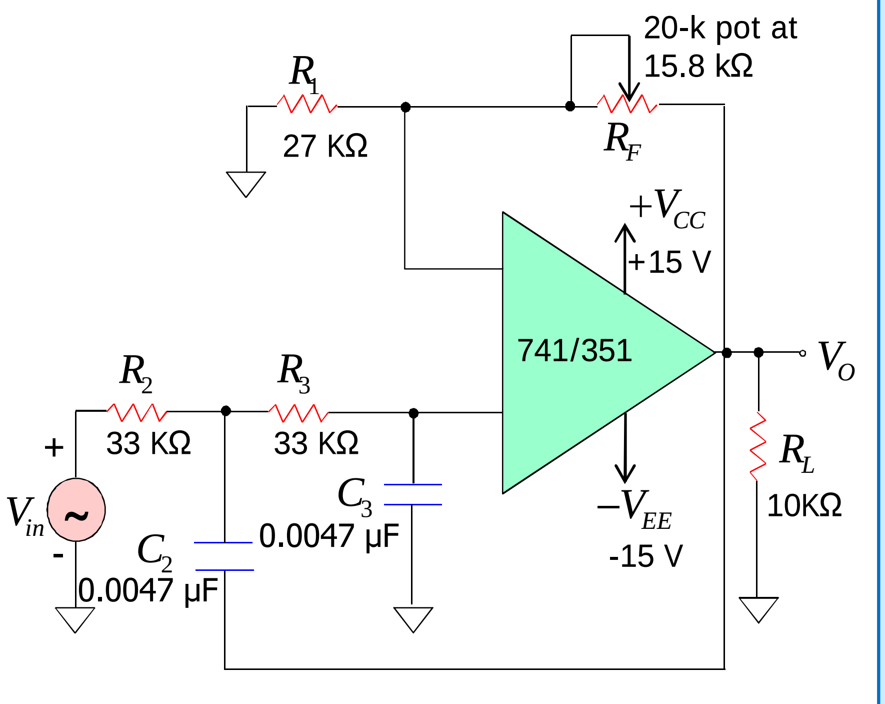
$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| < A_F$$

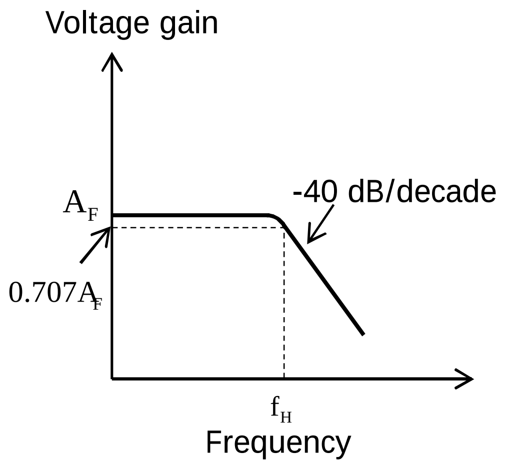


Problem

- Design a low pass filter at a cut off frequency of 1 kHz with a pass band gain of 2

Second order low pass butterworth filter





$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$$

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

$$A_F = 1+\frac{R_F}{R_1} = \text{passband gain of the filter}$$

$$f = \text{frequency of the input signal (Hz)}$$

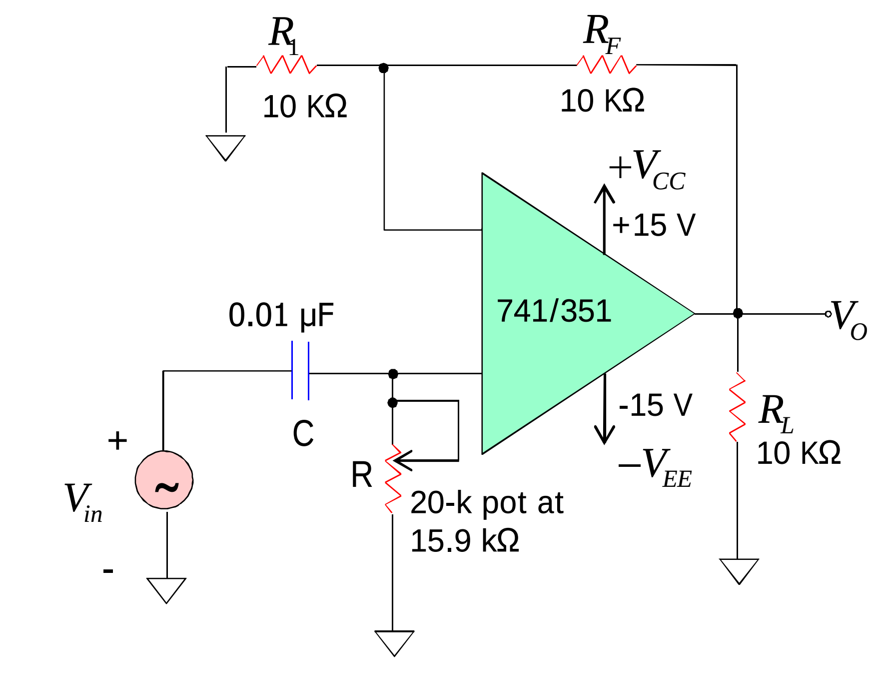
$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \text{high cutoff frequency (Hz)}$$

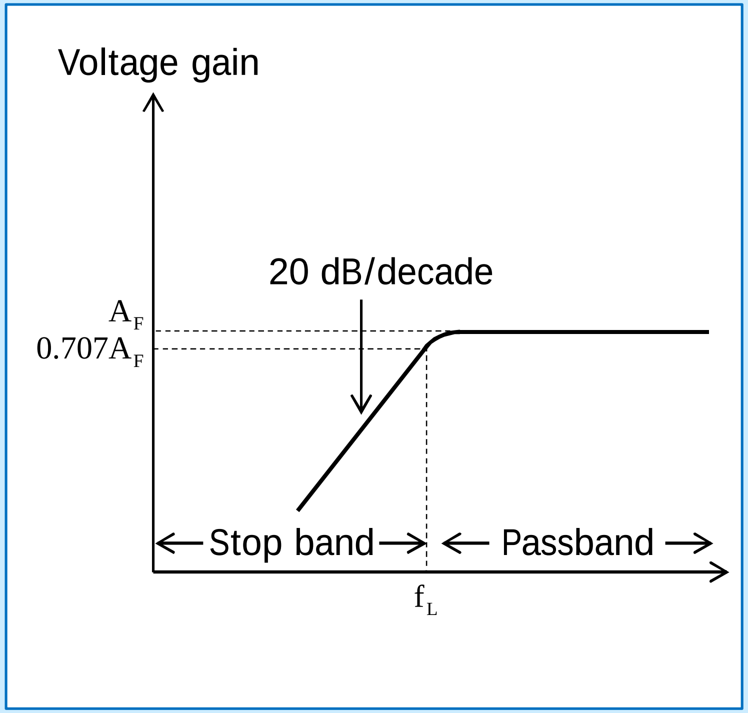
Gain for butterworth response = 1.586

Problem

- Design a second order low pass filter at high cutoff frequency of 1 kHz.

First order high-pass butterworth filter





$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = A_F\left[\frac{j(f/f_L)}{1+j(f/f_L)}\right]$$

$$A_F = 1+\frac{R_F}{R_1} = \text{passband gain of the filter}$$

$$f = \text{frequency of the input signal (Hz)}$$

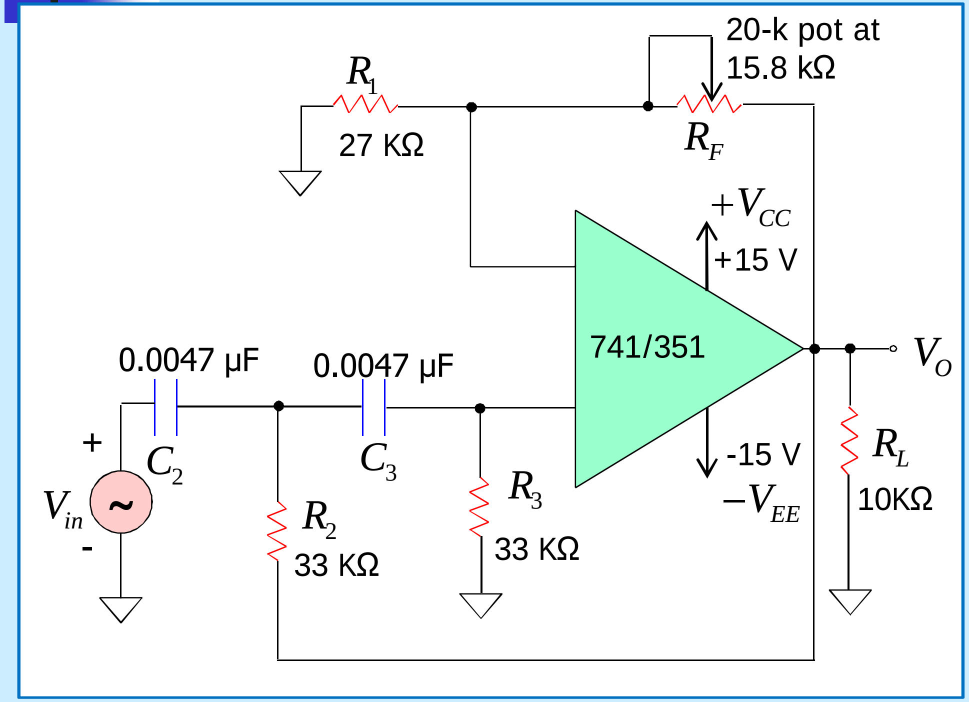
$$f_L = \frac{1}{2\pi RC} = \text{low cutoff frequency (Hz)}$$

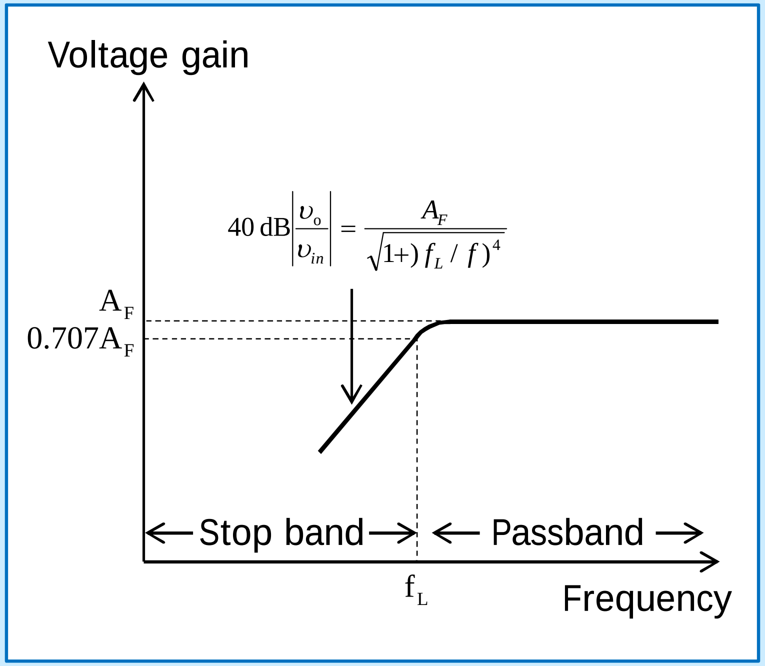
$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = \frac{A_F(f/f_L)}{\sqrt{1+(f/f_L)^2}}$$

Problem

Design a high-pass filter at cutoff frequency of 1 kHz with a pass-band gain of 2

Second order high-pass butterworth filter



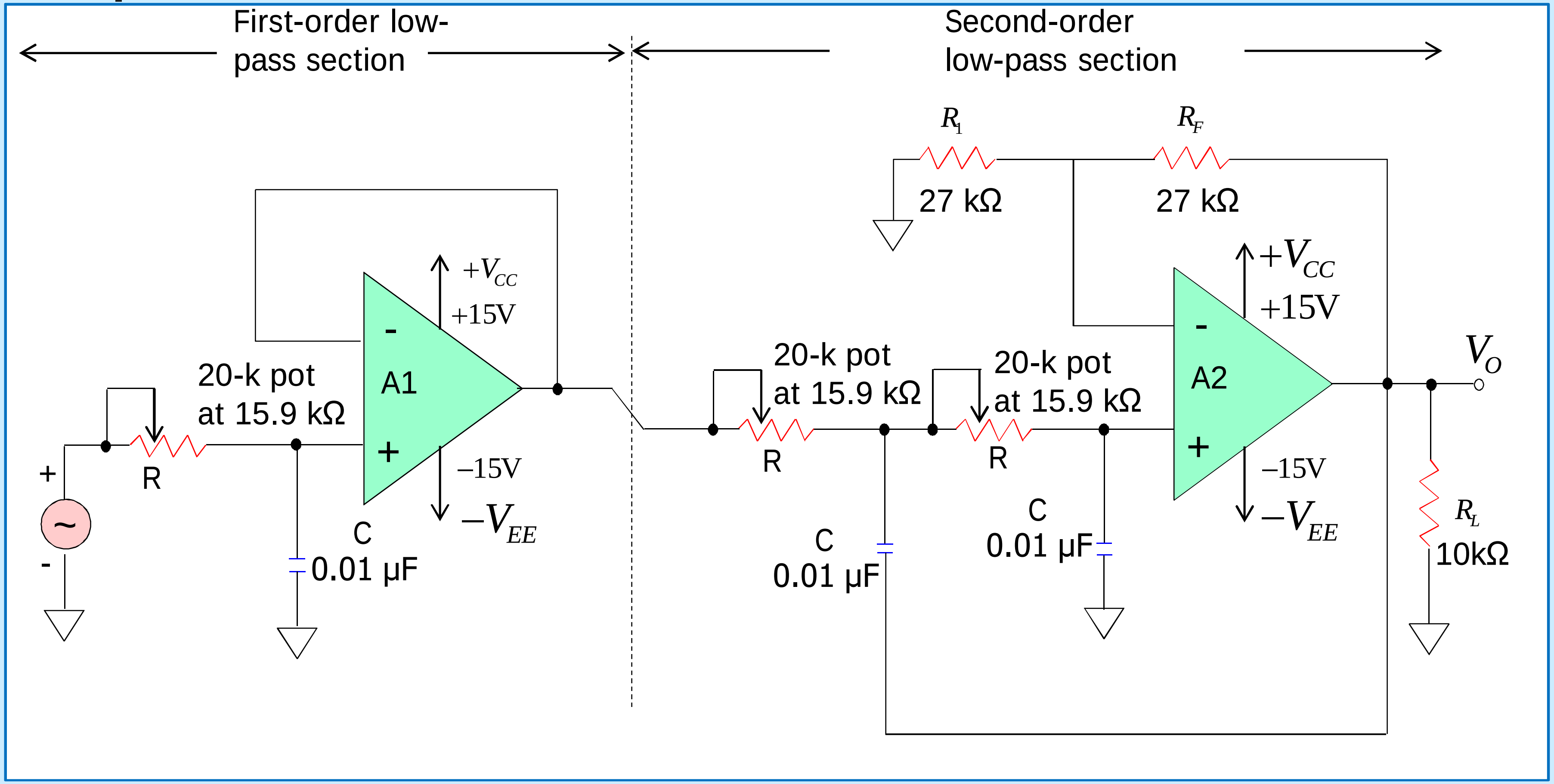


$$Where\ A_F = 1.586 = \text{Passband gain for the second order Butterworth}$$

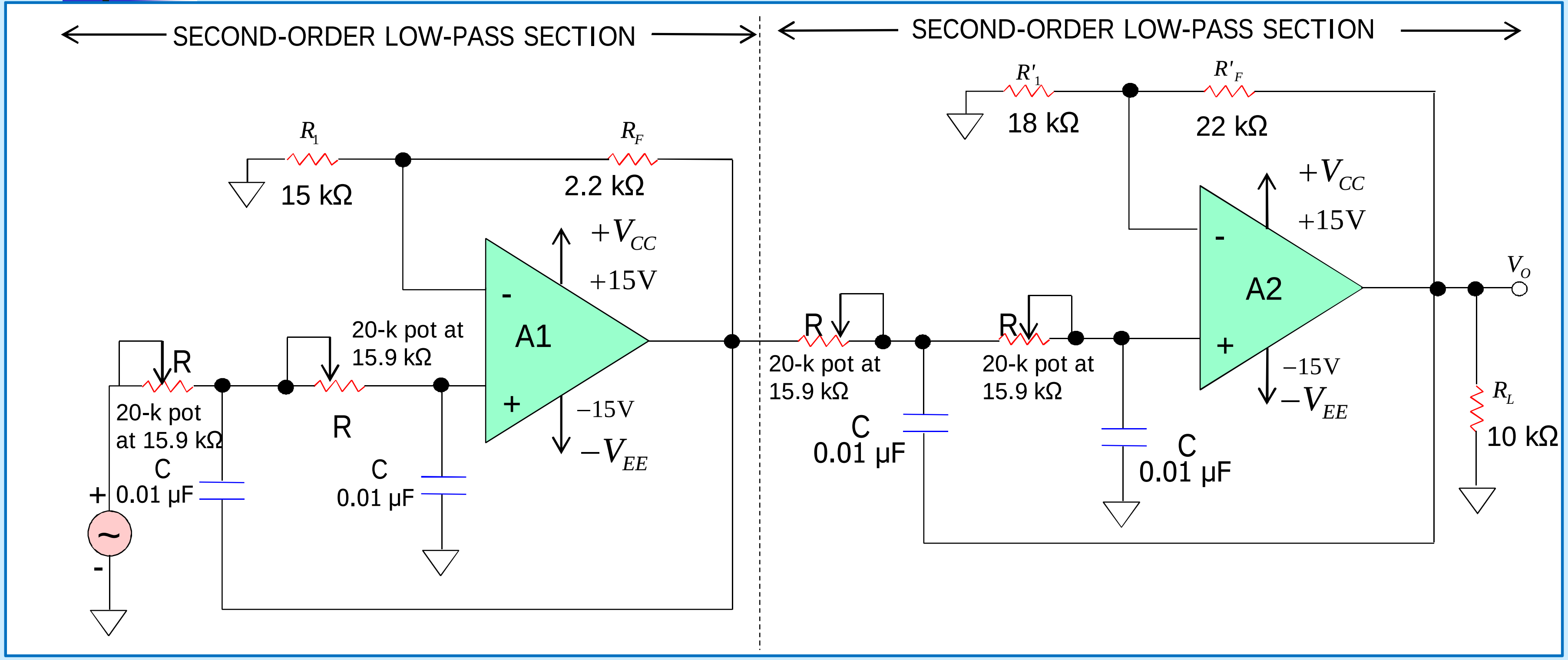
$$f = \text{frequency of the input signal (Hz)}$$

$$f_L = \text{low cutoff frequency (HZ)}$$

Higher order filter: Third order low pass

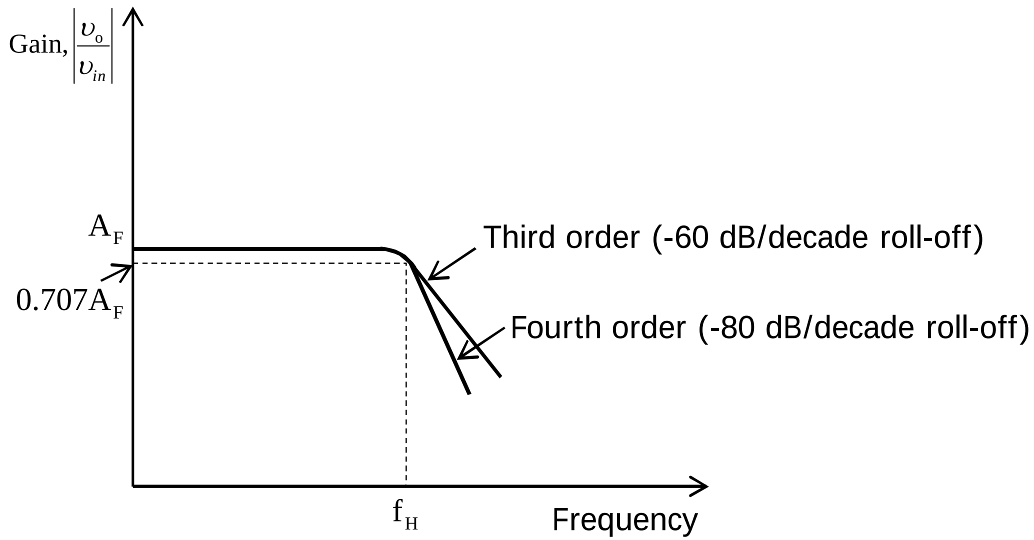


Fourth order low pass



- Size increase
- accuracy decrease
- gain fixed limitation

Contd.



Gain, $\left|\frac{\upsilon_o}{\upsilon_{in}}\right|$
A_F
$0.707A_F$
Third order (-60 dB/decade roll-off)
Fourth order (-80 dB/decade roll-off)
f_H
Frequency

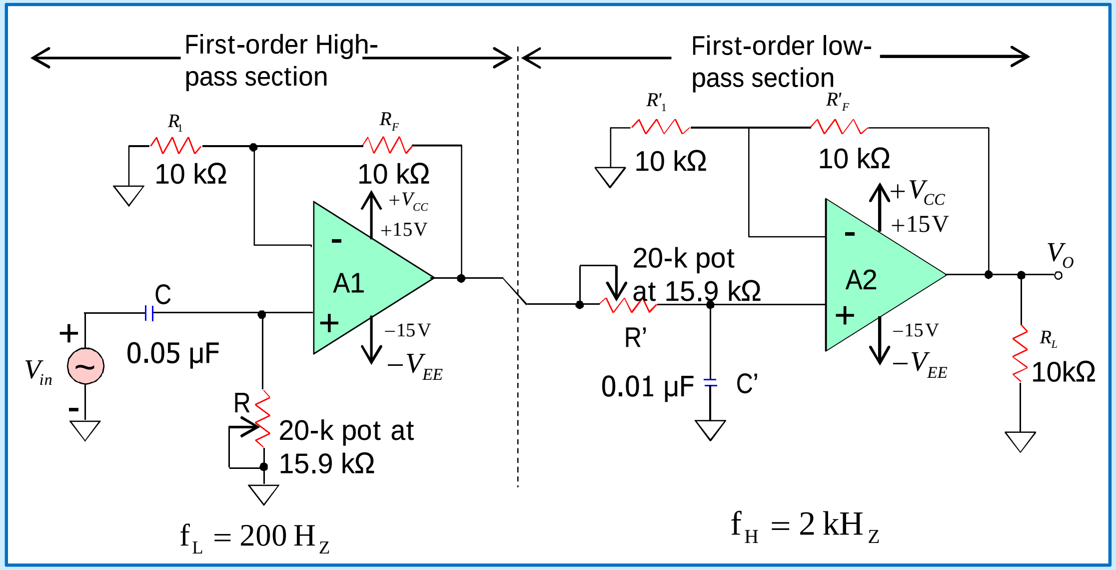
Band pass filter

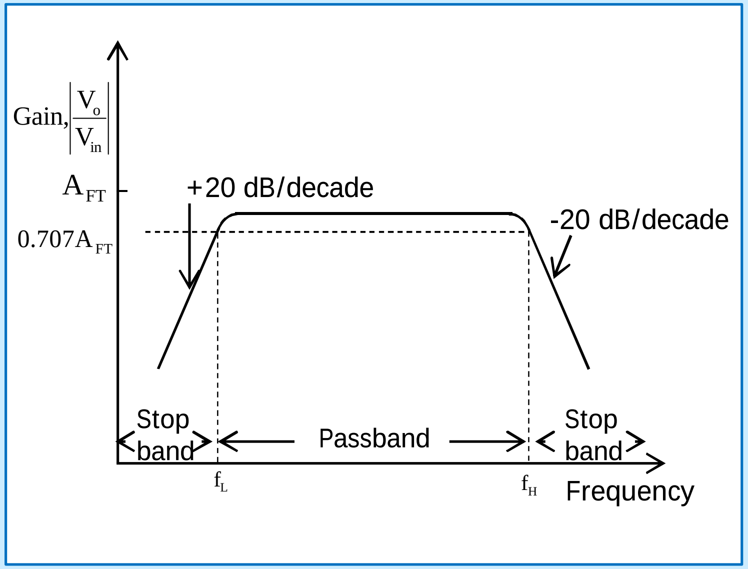
- Two types (based on Q factor)
  - Wide band pass (Q<10)
  - Narrow band pass (Q>10)

$$\boxed{Q = \frac{f_C}{BW} = \frac{f_C}{f_H - f_L}}$$

$$\boxed{f_C = \sqrt{f_H f_L}}$$

Wide band-pass filter

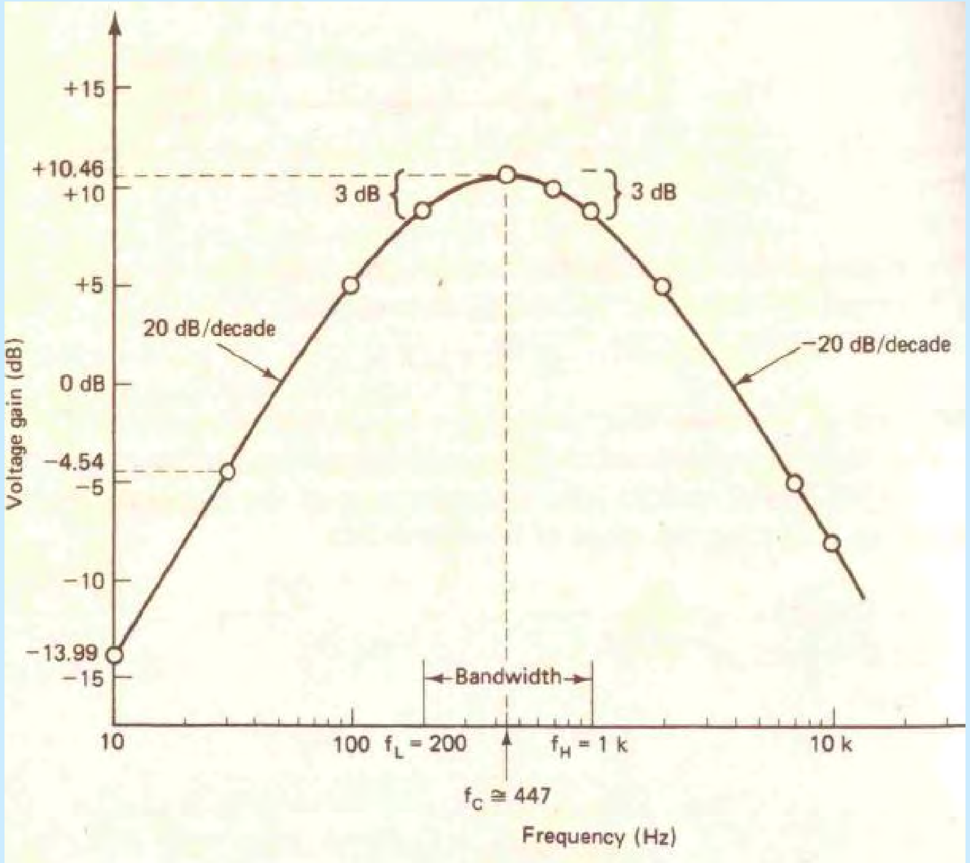




$$\left|\frac{\upsilon_o}{\upsilon_{in}}\right| = \frac{A_{FT}(f/f_L)}{\sqrt{[1+(f/f_L)^2][1+(f/f_H)^2]}}$$

Problem

Design a wide band-pass filter with $f_L = 200$ Hz and $f_H = 1$ KHz, and a pass band gain of 4. calculate value of Q for the filter.



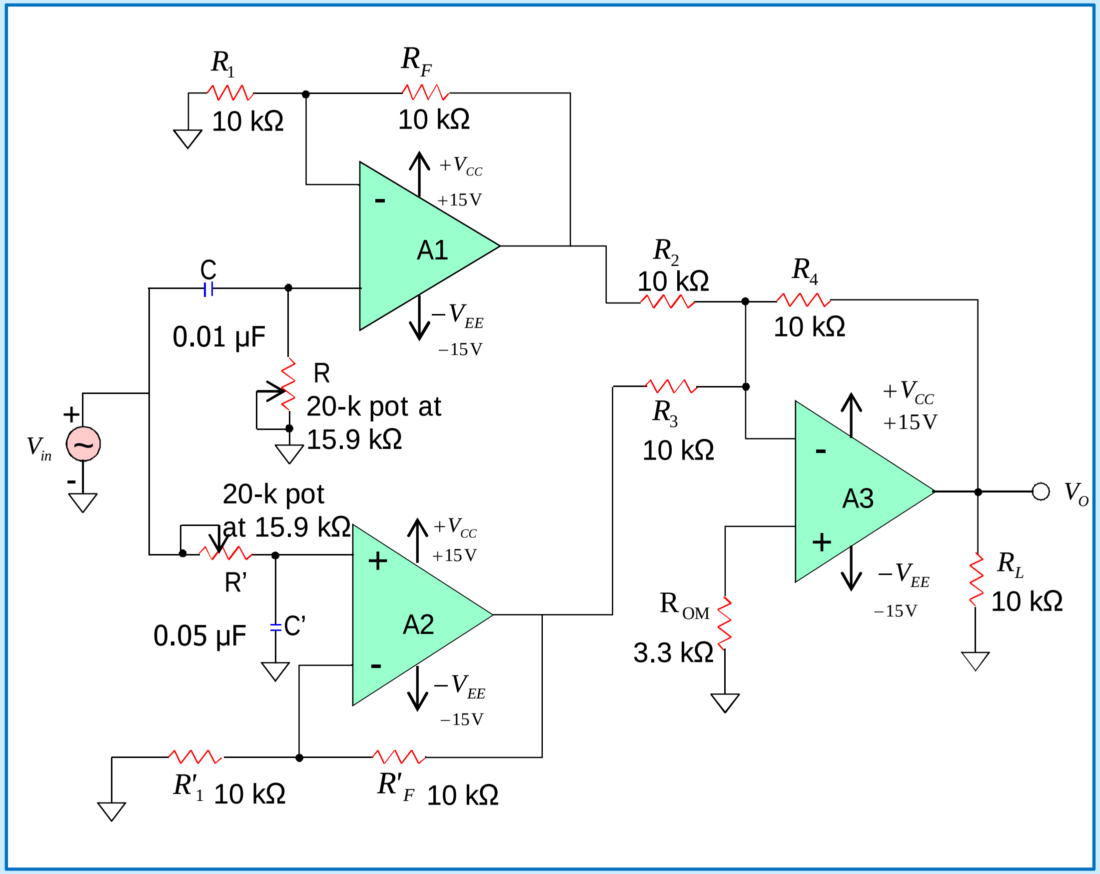
Band reject filter

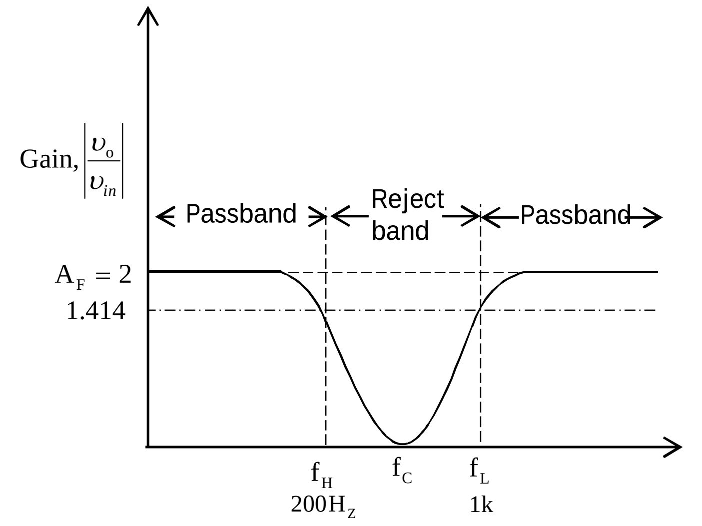
- Two types (based on Q factor)
  - Wide band reject (Q<10)
  - Narrow band reject (Q>10) (notch filter)

$$Q = \frac{f_C}{BW} = \frac{f_C}{f_H - f_L}$$

$$f_C = \sqrt{f_H f_L}$$

Contd.





$f_C = \sqrt{f_H f_L} = 447.2\,H_Z$

Wide band reject filter requirement

- Low cut of frequency of high pass filter must be larger than high cutoff frequency of low pass filter
- Pass band gain of both high pass and low pass must be equal

Problem

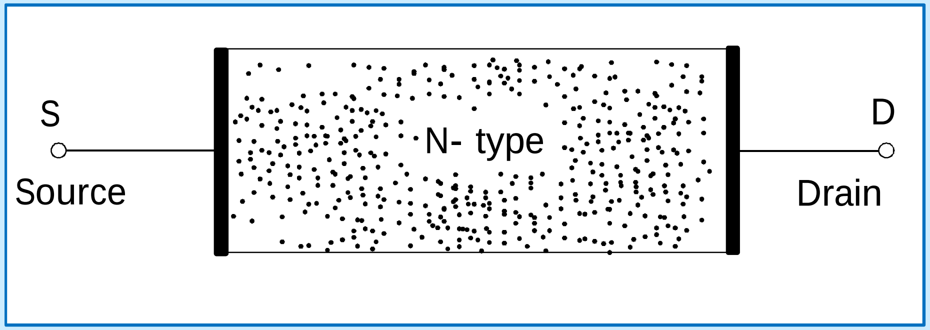
Design a wide band reject filter with f_L= 1 kHz and f_H = 200 Hz

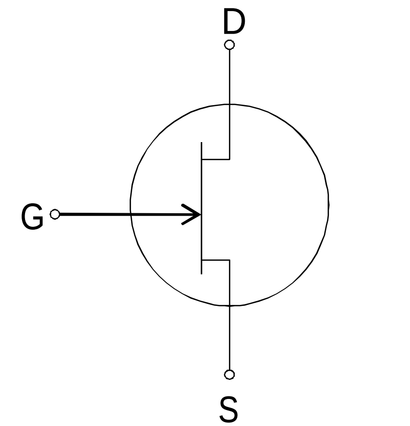
Field Effect Transistor (FET)

Introduction

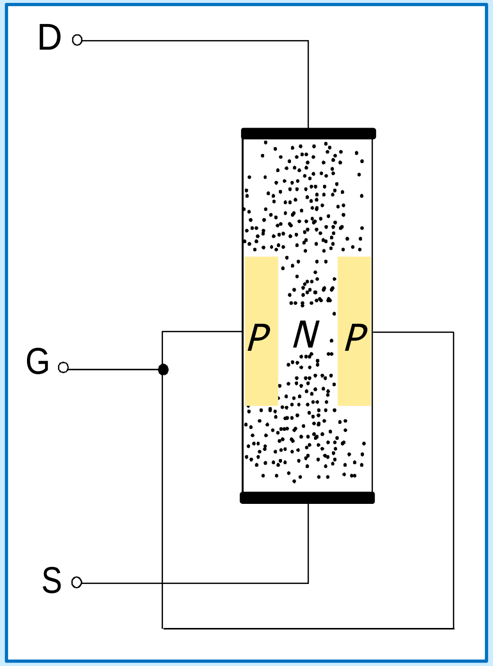
- Developed in 1960's
- Operation depend on majority carrier (unipolar transistor)
- Category
  - Junction FET (JFET)
  - Insulated gate FET (IGFET)
  - Metal oxide semiconductor (MOSFET)
- Advantages
  - High input impendence (~100 M ohm typical), where BJT typical value 2 k ohm
  - Easier to fabricate (suited for IC's)
  - Provide greater thermal stability compared to BJT
  - Less noisy than BJT and thus more suitable for input stage of low level amp.
  - Relatively immune to radiation, but BJT is very sensitive
- Disadvantage
  - Small Gain-bandwidth of device compared to BJT
  - Greater susceptibility to damage in handling

JFET

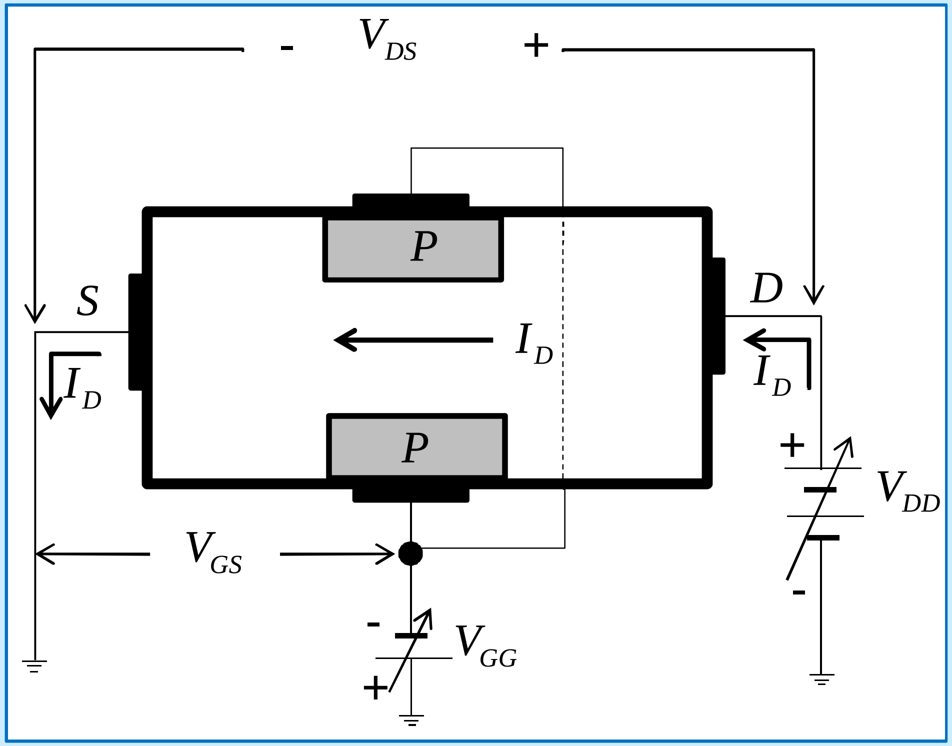


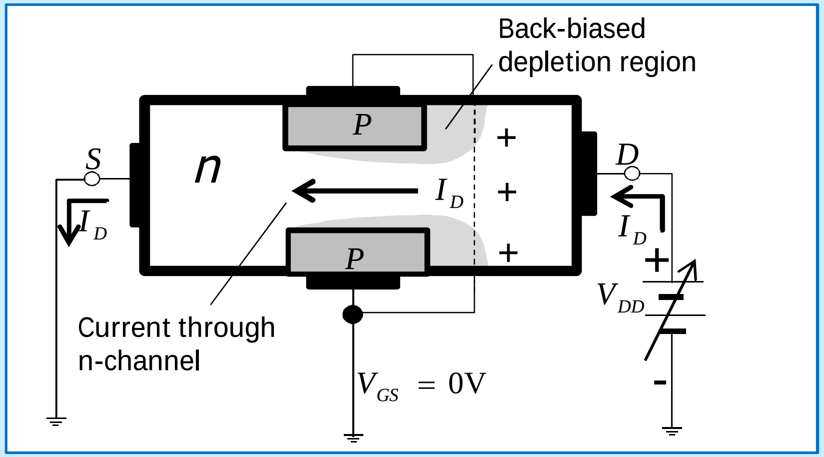


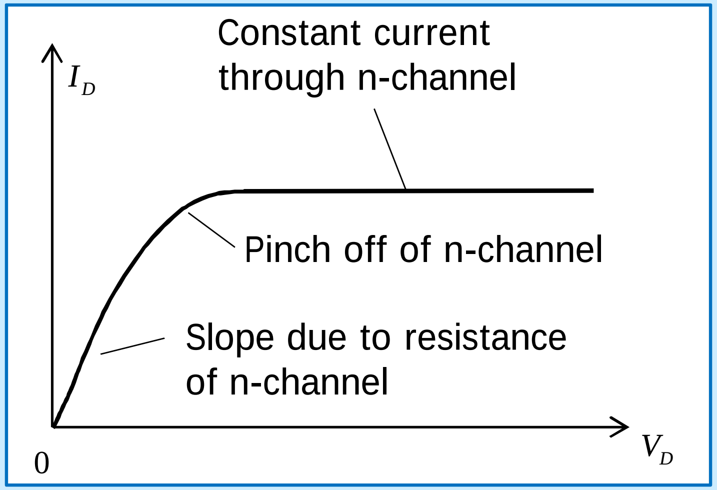
N- Channel, JFET



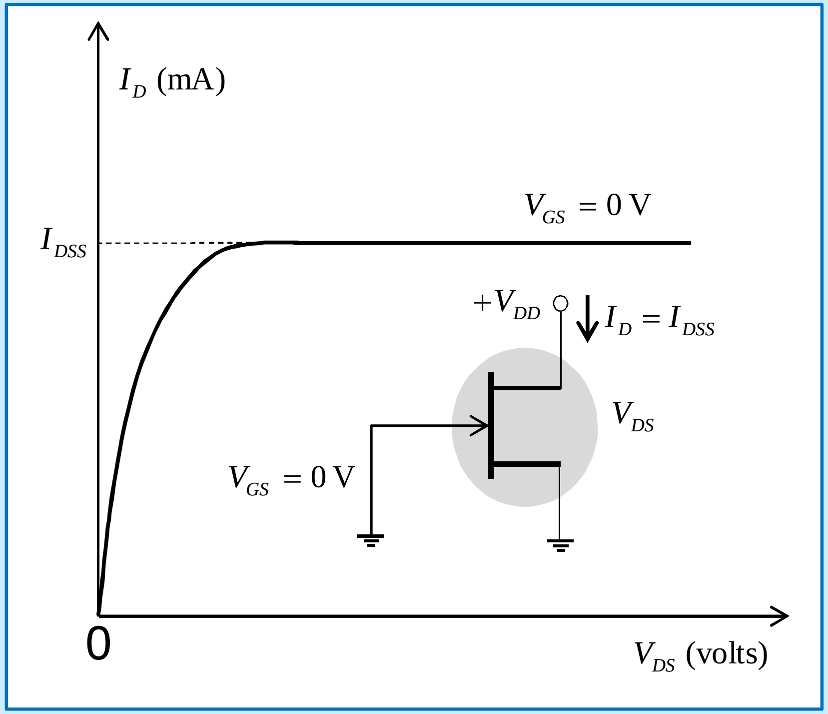
JFET biasing

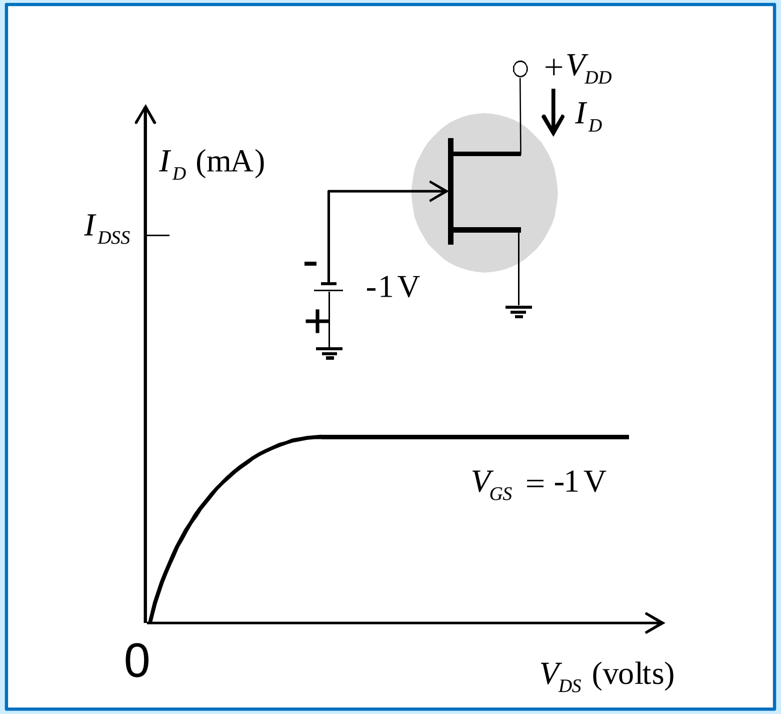






Drain source characteristics





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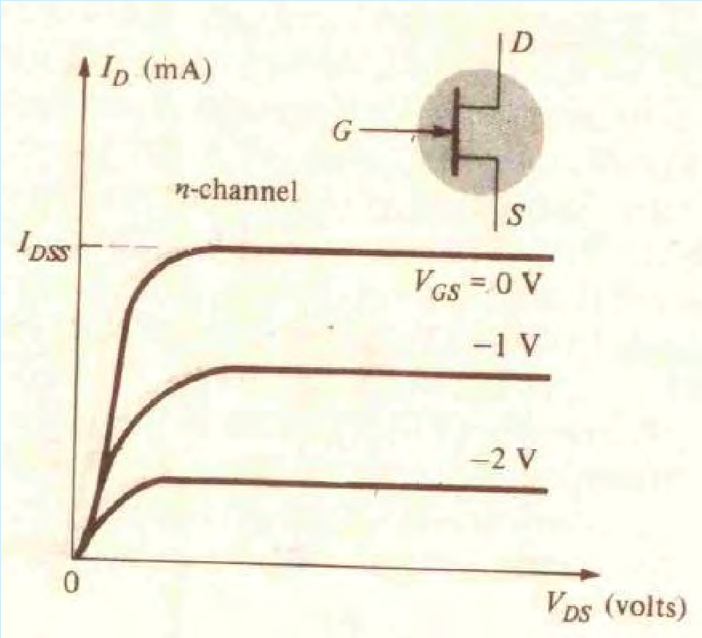
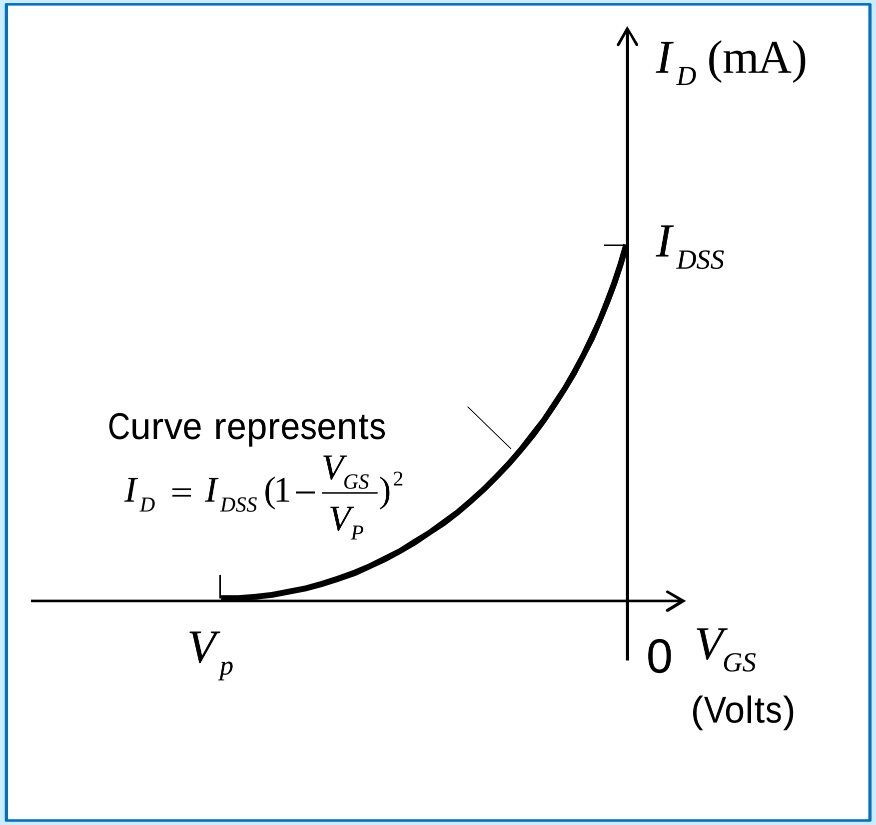


Transfer characteristics



$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$V_{GS} = 0 \text{ V}$

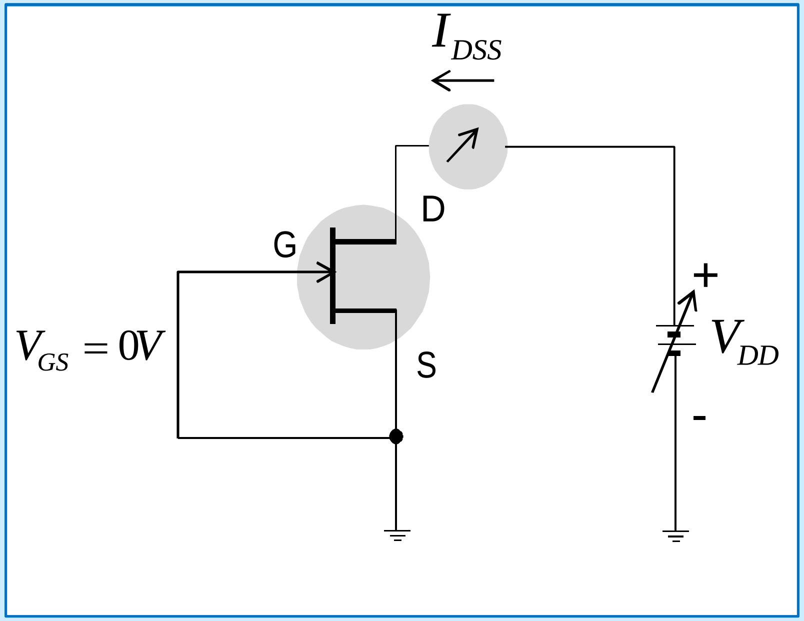
$I_D = I_{DSS}$

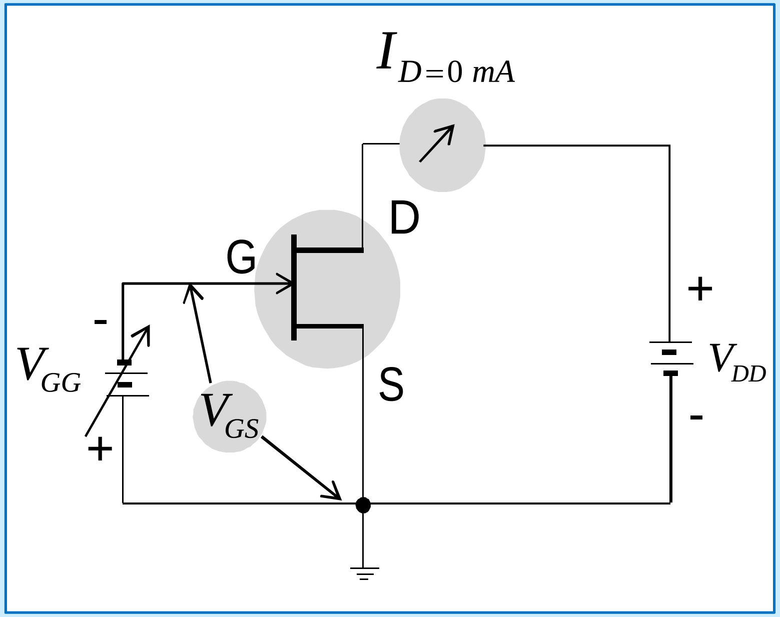
$I_D = 0, V_{GS} = V_P$

Problem

- Determine the drain current of an n-channel JFET having pinch off voltage Vp = -4 V and drain-source saturation current I_{DSS} =12 mA at the following gate-source voltages
  - V_{GS} = 0 V, -1.2 V and -2 V

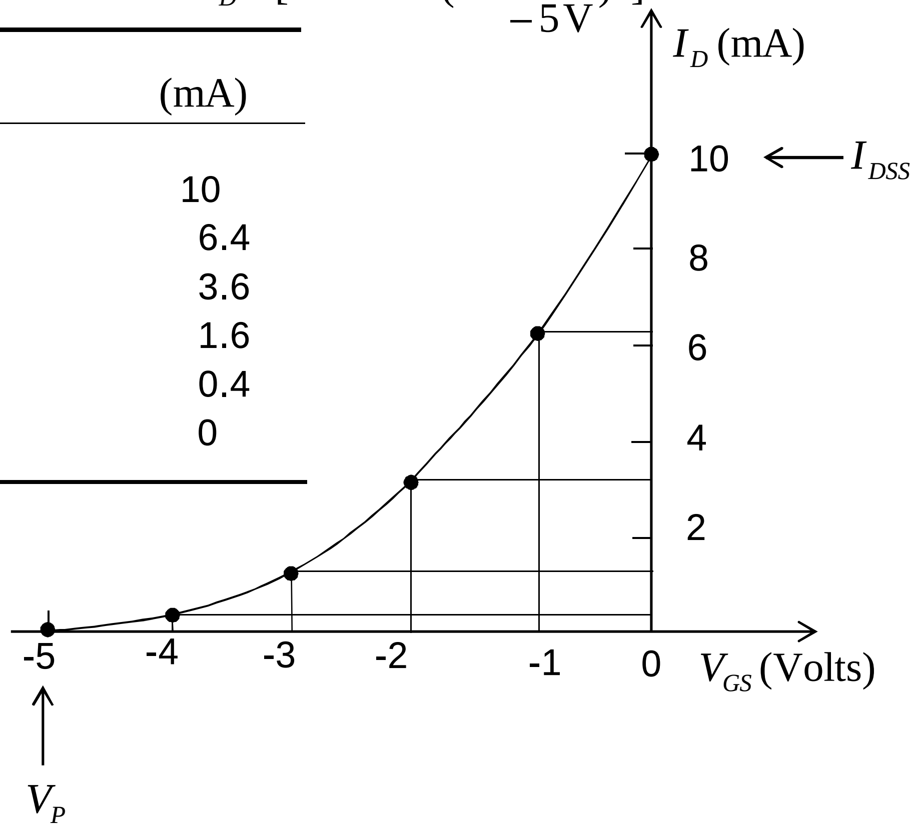
Plotting JFET Characteristics





Contd.

V_{GS} (V)	I_D (mA) $[= 10 \text{ mA}(1 - \frac{V_{GS}}{-5\text{V}})^2]$
0	10
-1	6.4
-2	3.6
-3	1.6
-4	0.4
-5	0



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$\frac{I_{DSS}}{2}$
$0.5V_P$	$\frac{I_{DSS}}{4}$
V_P	0

JFET Parameters

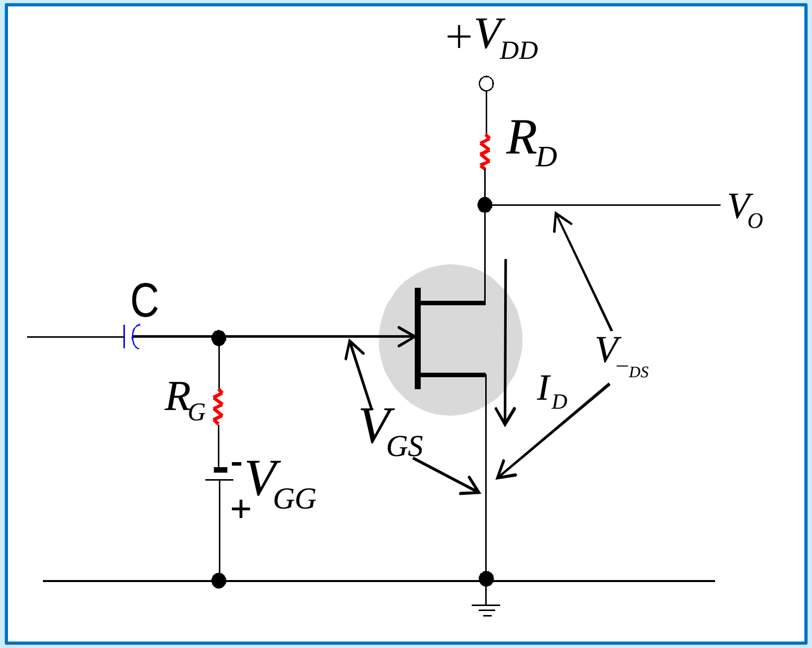
- Drain source saturation current (I_{DSS}) – current at which the channel pinch off when gate-source shorted ($V_{GS}=0$)
- Pinch-off voltage $V_P=V_{GS(off)}$ – gate source voltage at which drain source channel cut off or pinched off resulting no drain current
- Dynamic drain resistance (r_d): ratio of small change in drain voltage to the small change in drain current, keeping gate voltage constant

$$r_d = \left.\frac{\Delta \upsilon_{DS}}{\Delta i_D}\right|_{V_{GS} = \text{const}}$$

- Mutual conductance or transconductance (g_m): ratio of small change in drain current to the small change in gate voltage, keeping the drain voltage constant

$$g_m = \left.\frac{\Delta i_D}{\Delta \upsilon_{GS}}\right|_{V_{DS} = \text{const.}}$$

JFET Fixed Biasing



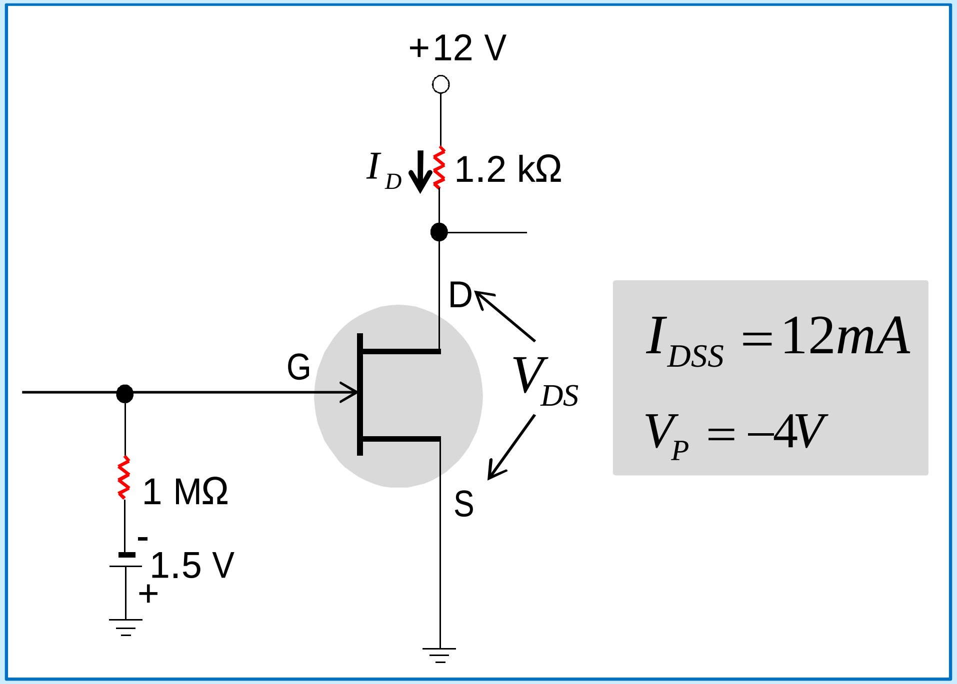
$$V_{GS} = V_G - V_S = V_{GG} - 0 = V_{GG}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

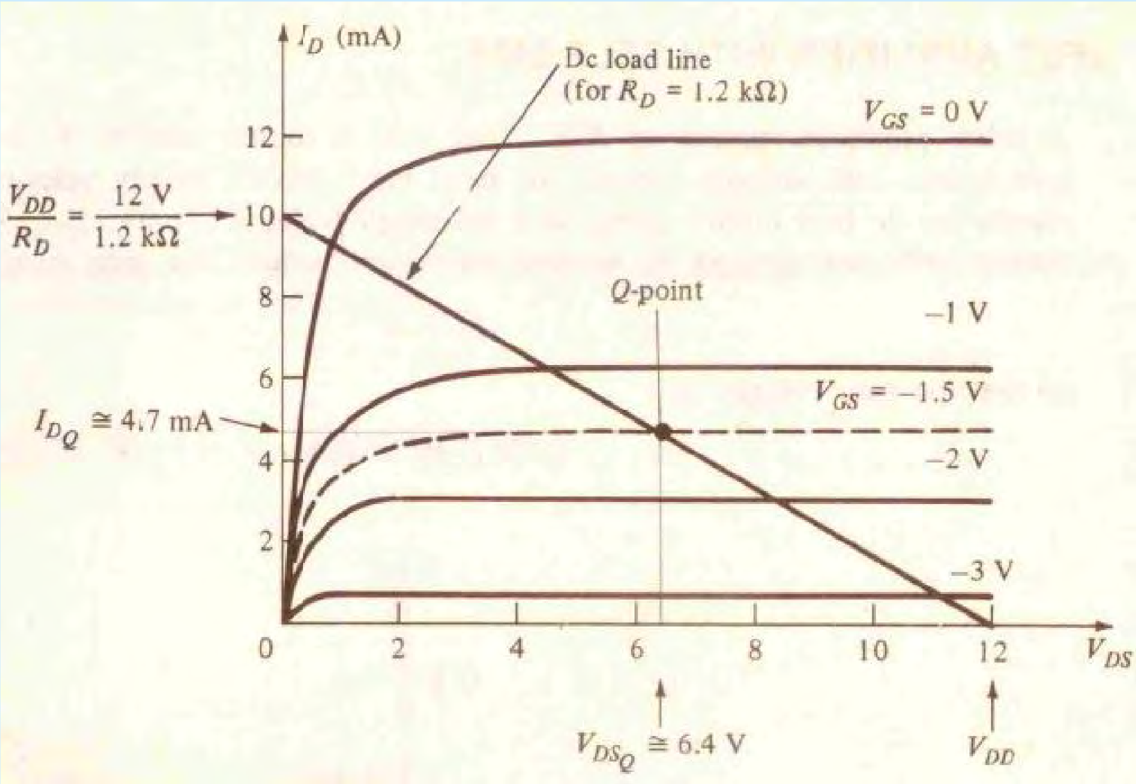
$$V_D = V_{DD} - I_D R_D$$

Problem

- Find drain current and drain source voltage



Graphical approach



$$V_D = V_{DD} - I_D R_D$$

$$I_D = 0 \qquad V_D = V_{DD}$$

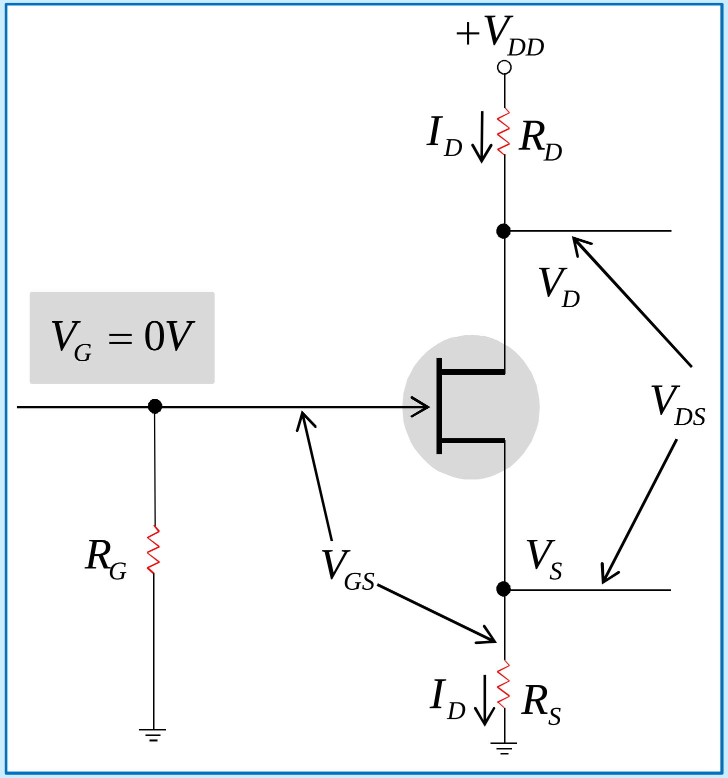
$$V_D = 0\ \text{V}$$

$$0\ \text{V} = V_{DD} - I_D R_D$$

$$I_D = \frac{V_{DD}}{R_D}$$

JFET with self bias

- With single supply voltage supply



$$I_G = 0$$

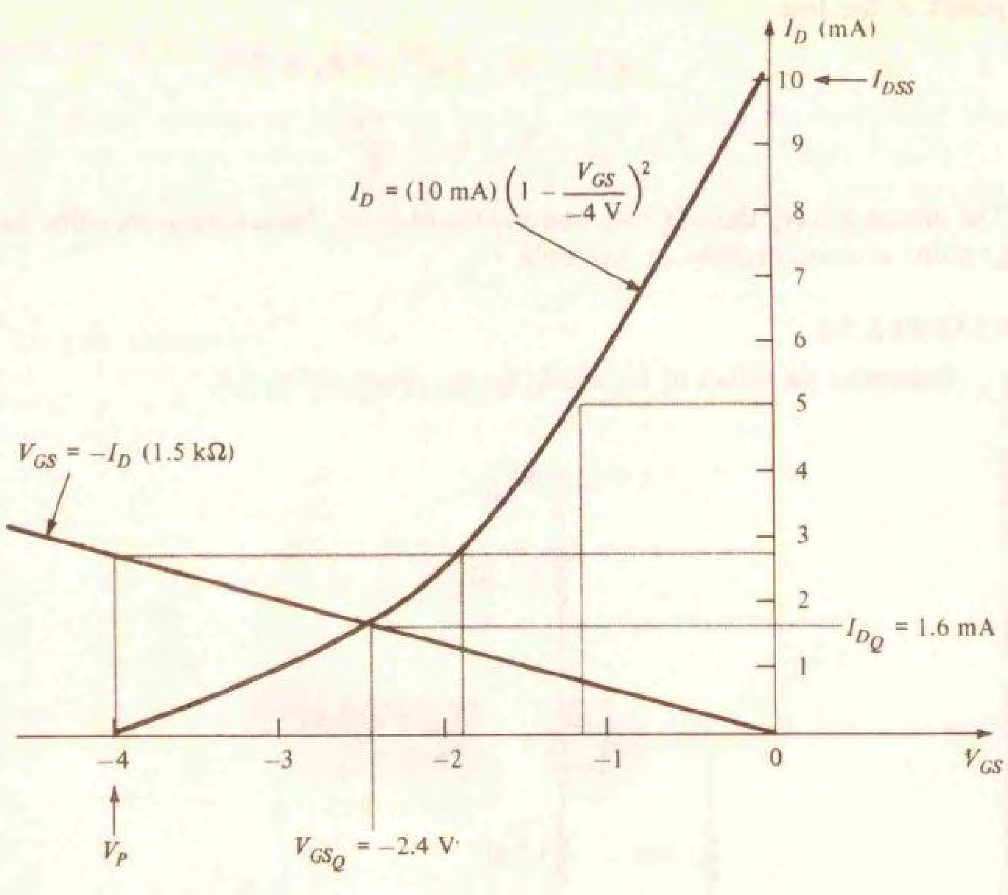
$$V_G = I_G R_G = 0 \text{ V}$$

$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S = 0 \text{ V} - I_D R_S$$

$$\boxed{V_{GS} = -I_D R_S}$$

Contd.

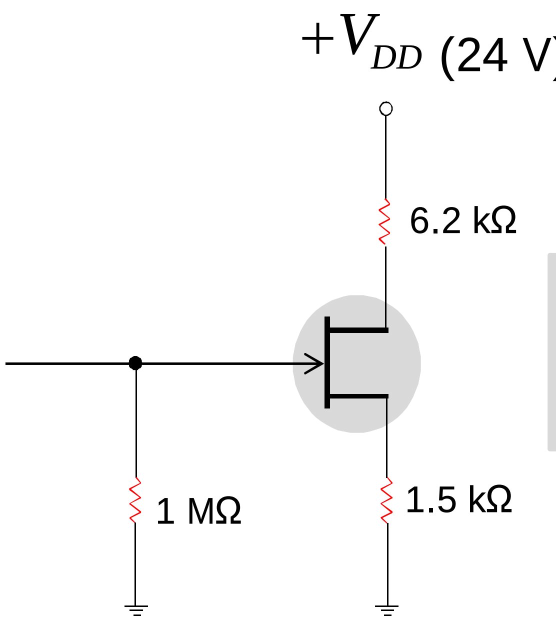


$$\text{For } \mathrm{I_D} = 0: \quad V_{GS} = (\mathrm{O})R_S = 0\ \mathrm{V}$$

$$\text{For } V_{GS} = V_P: \quad I_D = \frac{-V_P}{R_S}$$

Problem

- Determine the value of V_{GS} and I_D



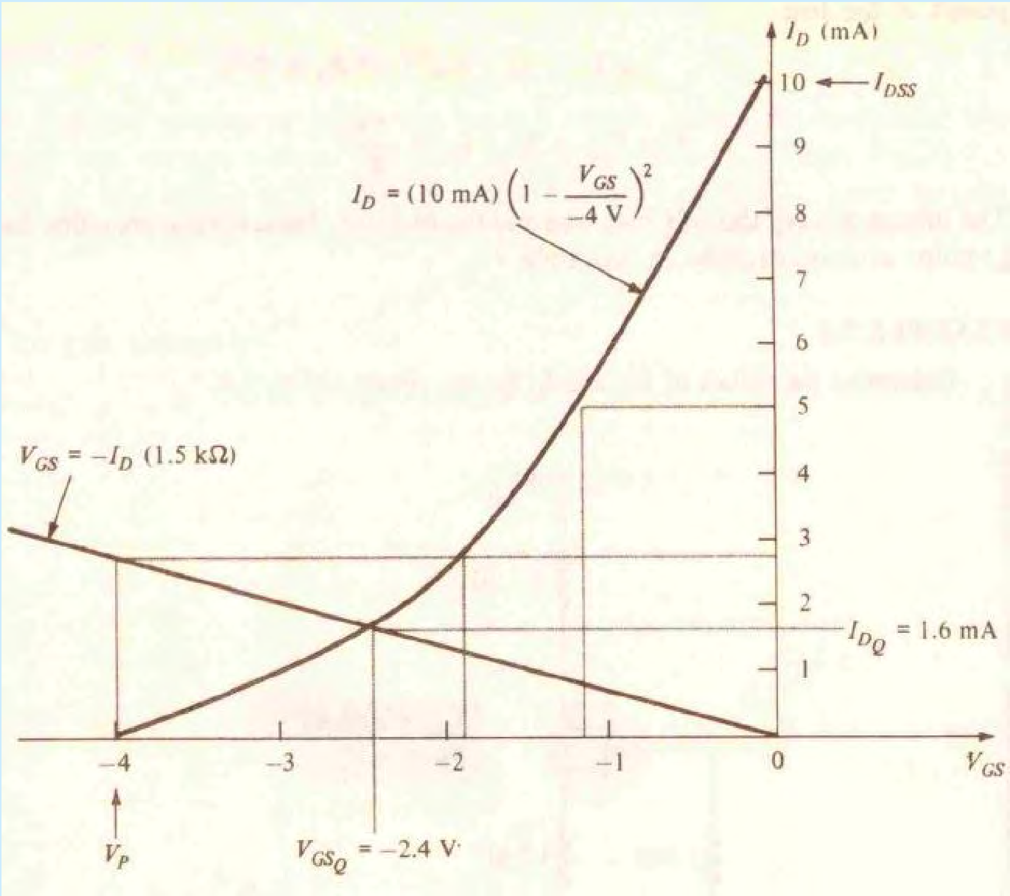
$$I_{DSS} = 10\,\text{mA}$$

$$V_P = -4\,\text{V}$$

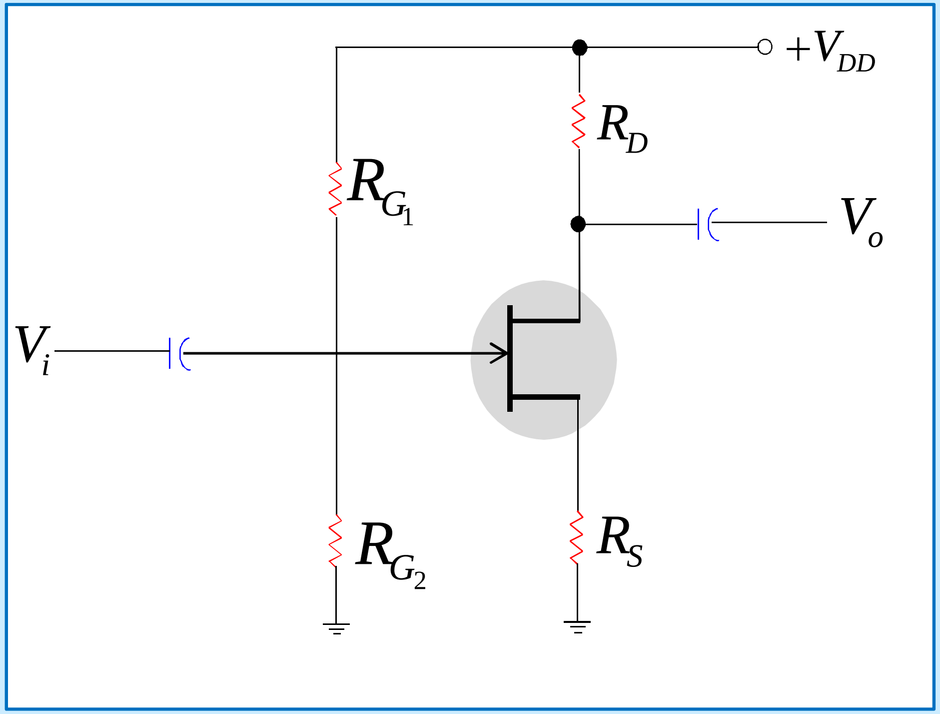
Ans

	V_{GS}(V)	I_D(mA)	
	0	10	
$[0.3V_P]$	-1.2	5	$\left[\frac{I_{DSS}}{2}\right]$
$[0.5V_P]$	-2.0	2.5	$\left[\frac{I_{DSS}}{4}\right]$
$[V_P]$	-4.0	0	

	I_D(mA)	V_{GS}(V)
	0	0
$\left[-\frac{V_P}{R_S}\right]$	2.67	-4



Voltage divider bias

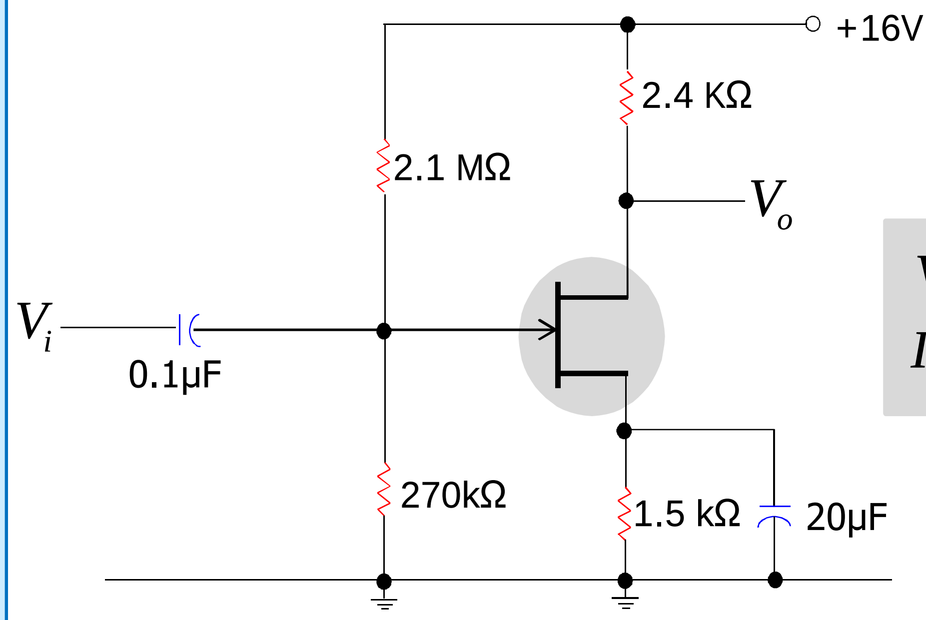


$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$$

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

Problem

- Determine the bias current in the circuit

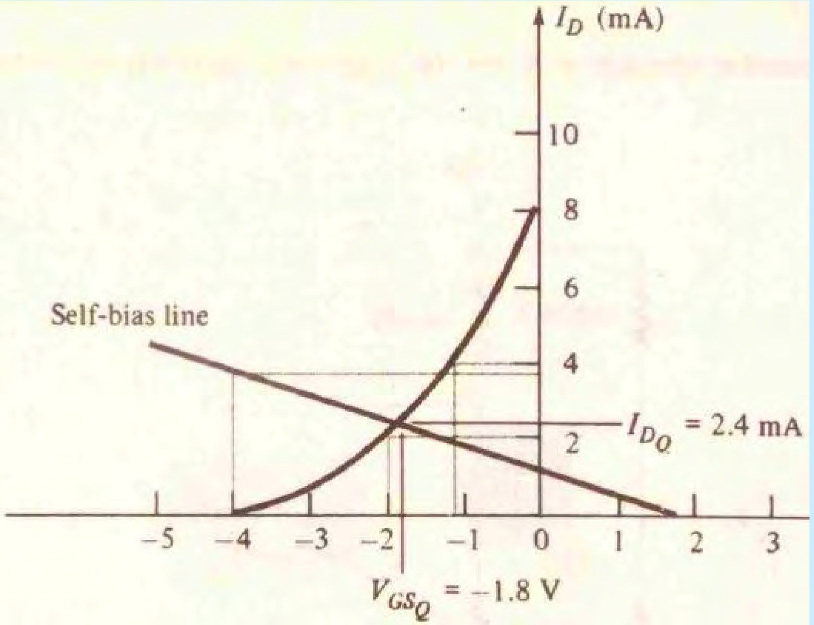


$V_P = -4\text{V}$

$I_{DSS} = 8 \text{ mA}$

Ans

V_{GS}(V)		I_D(mA)	
	0	8	
$[0.3V_P]$	-1.2	4	$\left[\frac{I_{DSS}}{2}\right]$
$[0.5V_P]$	-2	2	$\left[\frac{I_{DSS}}{4}\right]$
$[V_P]$	-4	0	



$$V_G = \frac{270\text{ k}\Omega}{2.1\text{ M}\Omega + 270\text{ k}\Omega}(16\text{V}) = +1.82\text{ V}$$

$$V_{GS} = 1.82\text{ V} - I_D(1.5\text{k}\Omega)$$

I_D=0, V_{GS} = -1.82V

$$\text{For } V_{GS} = 0: \quad I_D = \frac{-V_{GS}}{R_S} = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

I_D(mA)	V_{GS}(V)
0	1.82
1.21	0

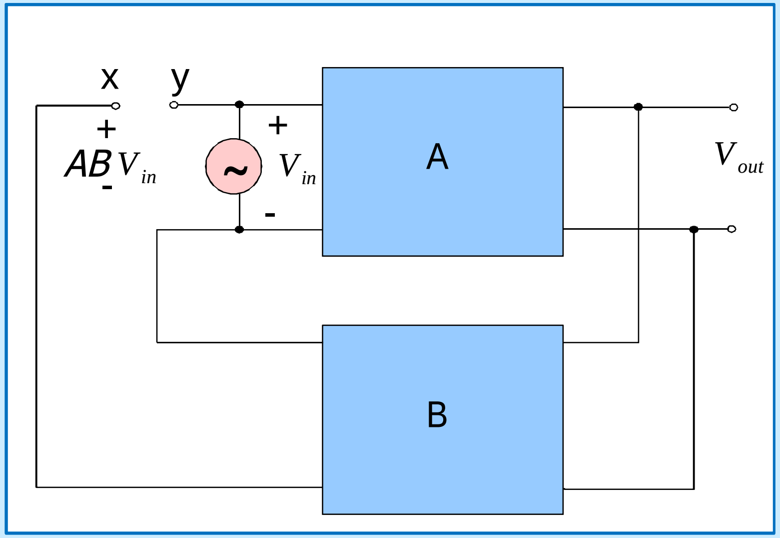
Oscillators

Sinusoidal oscillator

Oscillator is an amplifier which have positive feedback to supply own inputs voltage

Requirement

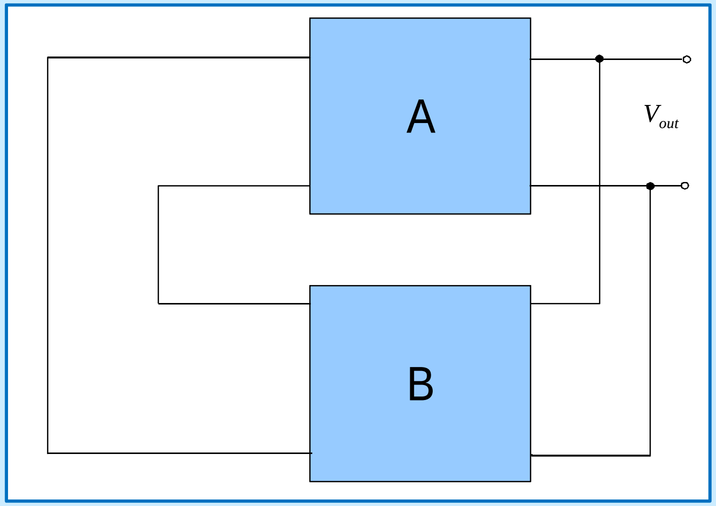
- Need a positive feedback (with a resonant circuit)
- Loop gain should be unity

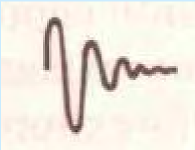


$V_{out} = A\ v_{in}$

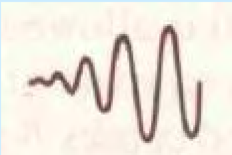
$V_f = AB\ v_{in}$

Contd.

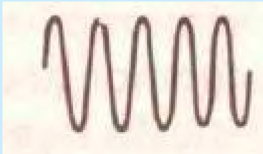




AB<1



AB>1



AB=1

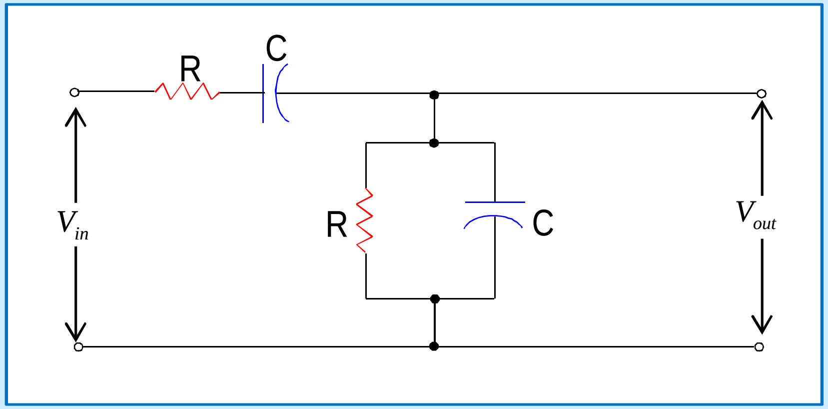
Initially, AB greater than one, as voltage build up, AB automatically decrease to 1

Starting Voltage : Noise

Wien bridge oscillator

- For low to moderate frequencies (5Hz to 1 M Hz)
- Uses a feedback circuit called lead leg network

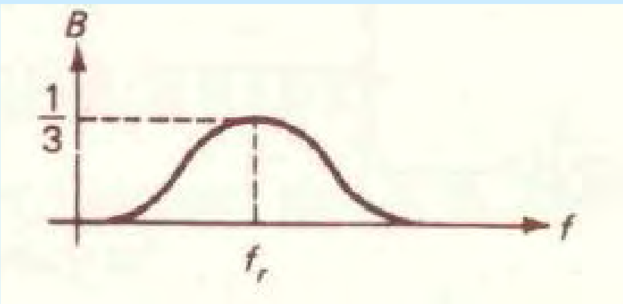
Lead-lag network

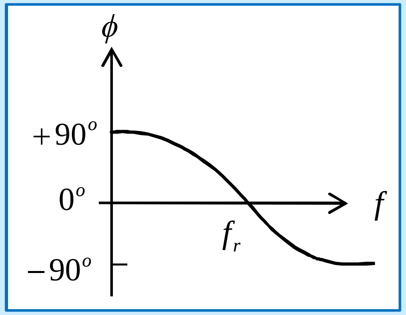


$$V_{out} = \frac{R||(-jX_C)}{R - jX_C + R||(-jX_C)} V_{in}$$

$$B = \frac{1}{\sqrt{9 + (X_C/R - R/X_C)^2}}$$

$$\phi = \arctan \frac{X_C/R - R/X_C}{3}$$





when $X_C = R$

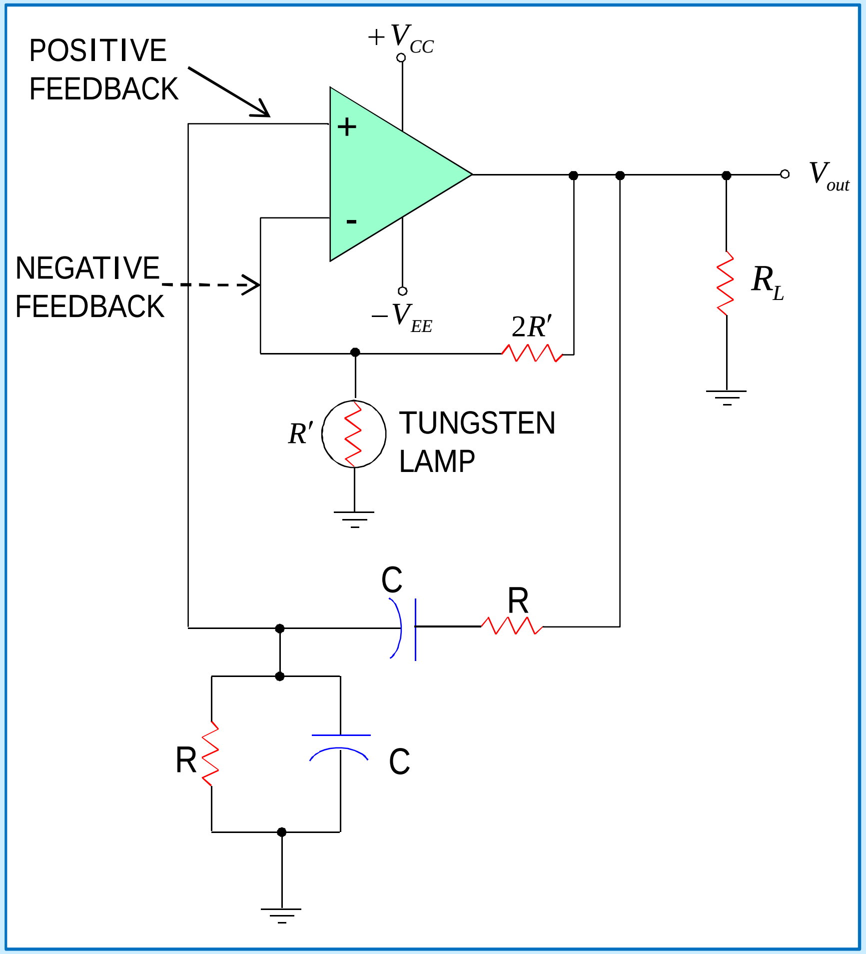
$$\frac{1}{2\pi frC} = R$$

$$fr = \frac{1}{2\pi RC}$$

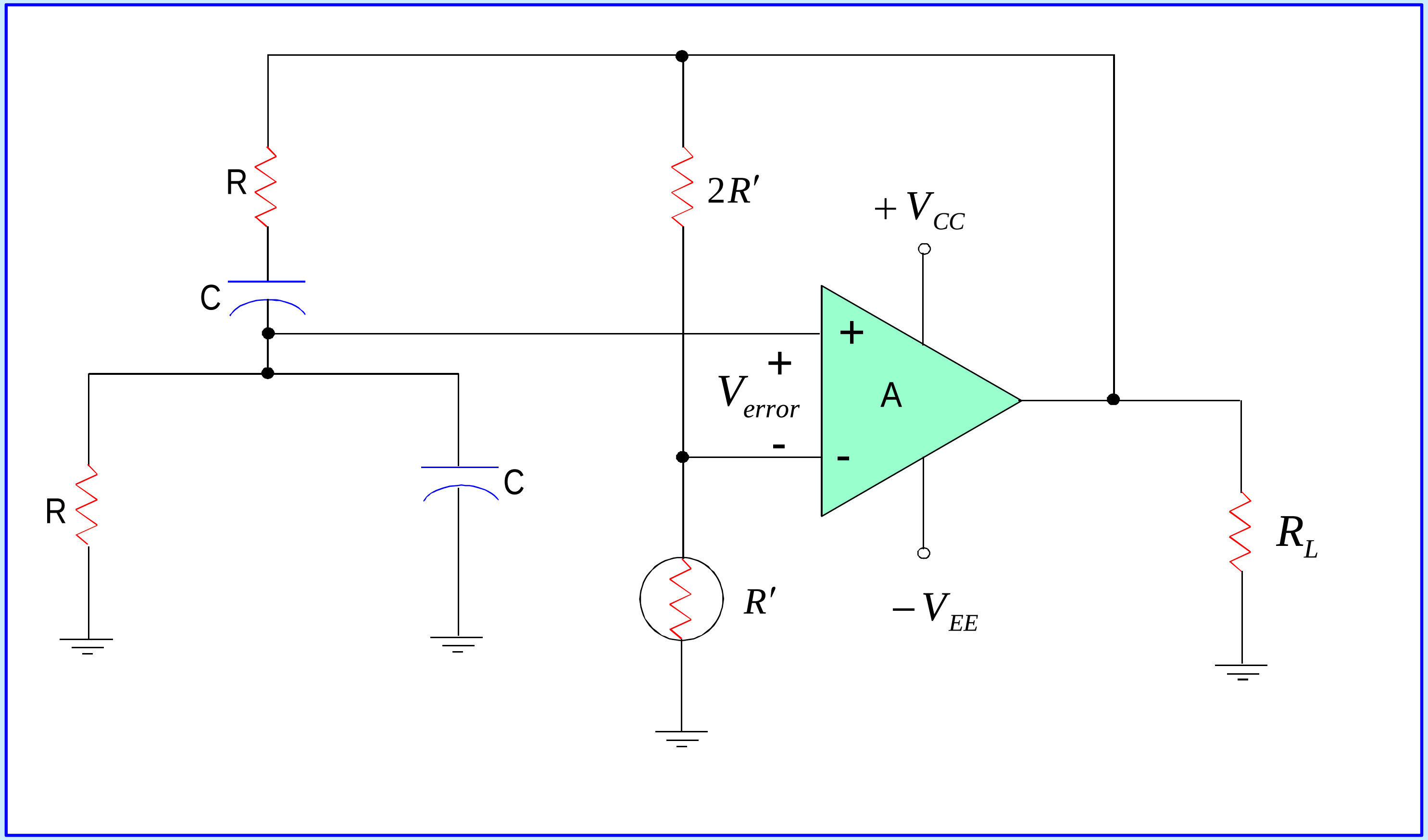
Practical circuit

- Initially tungsten lamp has low resistance
- As oscillation build up resistance increases and gain reaches to 3, then oscillation stabilize which stablize tungsten lamp resistance

$$A_{CL} = \frac{R_1}{R_2} + 1 = \frac{2R'}{R'} + 1 = 3$$



Bridge



Regulated Power Supplies

Introduction

Requirements

- Output voltage constant despite relatively large changes in line voltage and load current
- Temperature stability
- Variable level of voltages

Voltage feedback regulation

- Use Zener diode as reference
- Keep the voltage constant even input voltage and load current change due to feedback mechanism

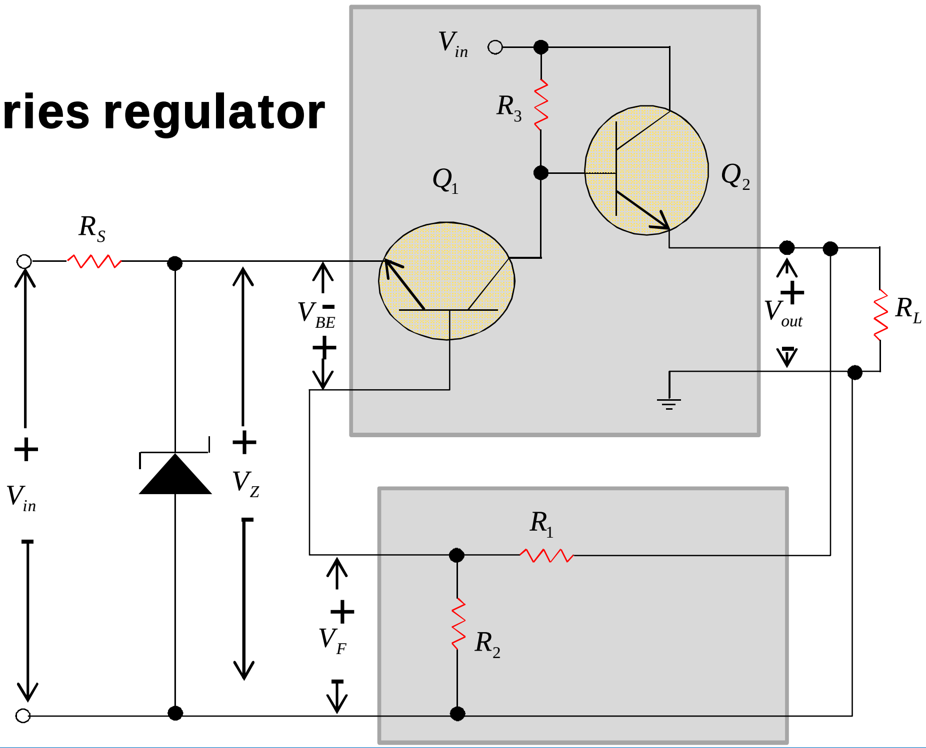
$$B \cong \frac{R_2}{R_1 + R_2}$$

$$V_F = V_Z + V_{BE}$$

$$BV_{out} = V_Z + V_{BE}$$

$$V_{out} = \frac{V_Z + V_{BE}}{B}$$

Series regulator



V_Z = zener voltage

V_{BE} = base-emitter voltage of Q_1

V_{out} = regulated output voltage

Power dissipation in pass transistor

$$\boxed{P_D = V_{CE} I_C}$$

$$\boxed{V_{CE} = \text{collector} - \text{emitter voltage},\ V_{in} - V_{out}}$$

$$\boxed{I_C = \text{load current plus divider current}}$$

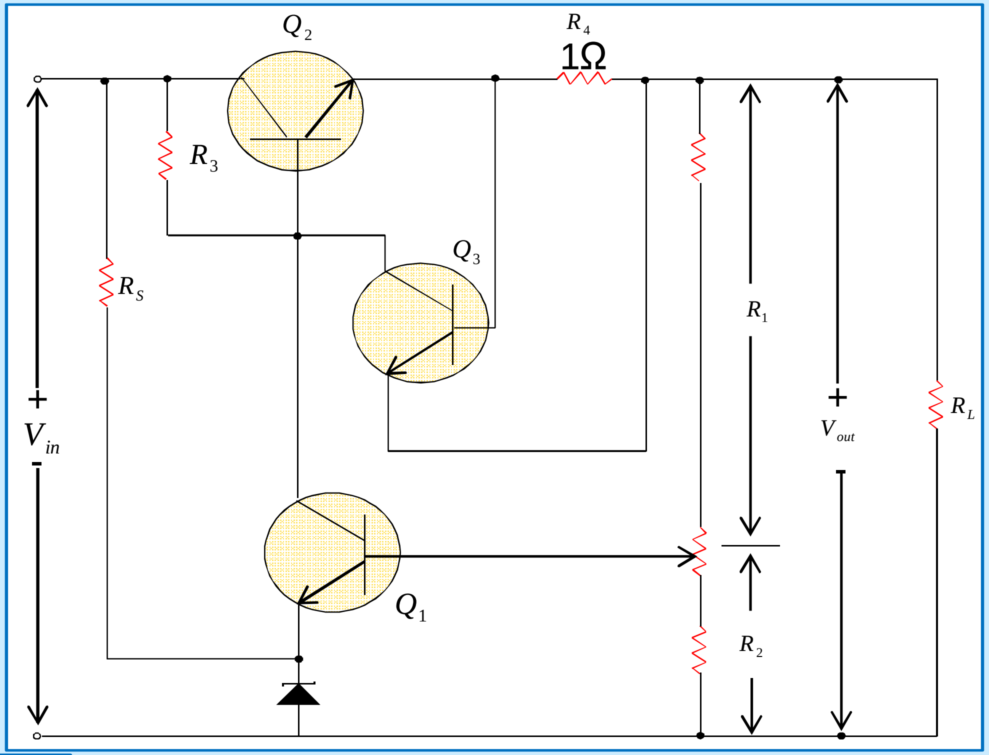
- When load current is heavy pass transistor has to dissipate lot of power
- Sometime cooling is required

Current limiting

- Series regulator has no short circuit protection
- If accidently short the load terminals, we get an enormous load current that will destroy the pass transistor or a diode

$$V_{BE} = I_{SL} R_4$$

$$I_{SL} = \frac{V_{BE}}{R_4}$$



where I_{SL} = short – circuit load current

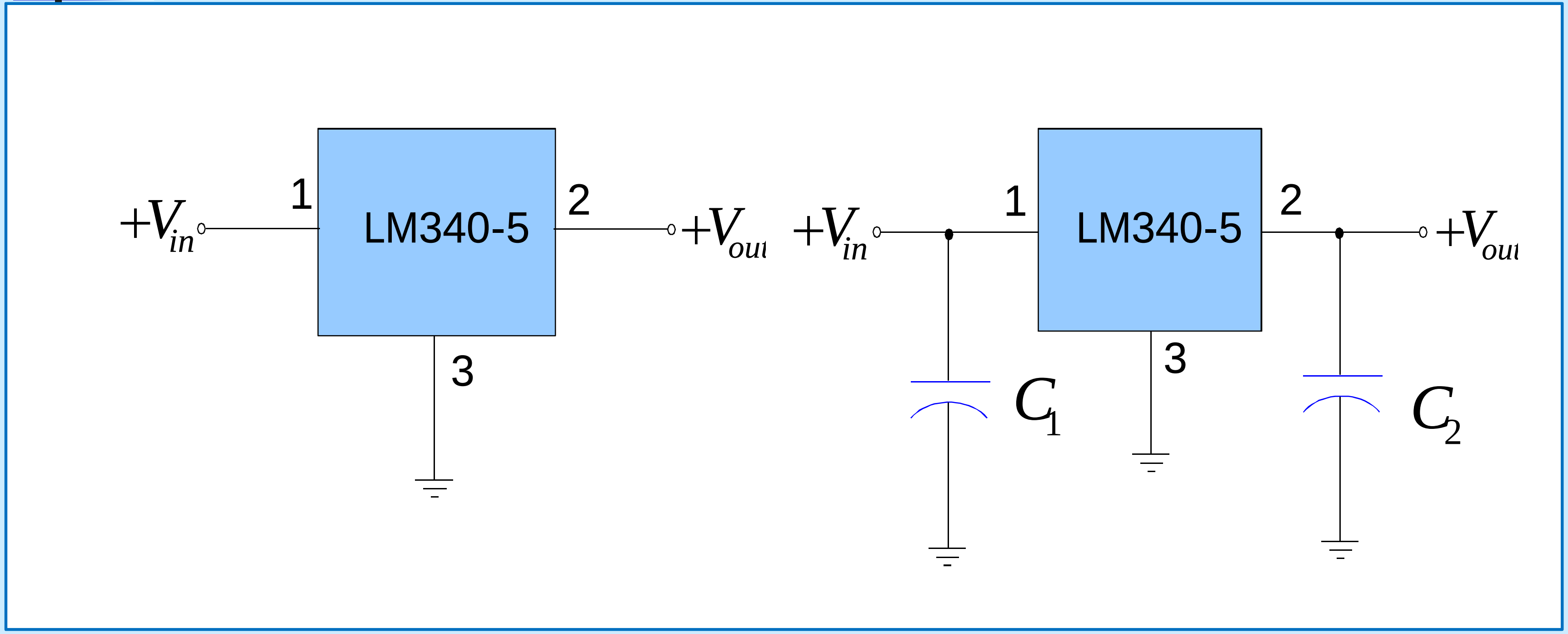
V_{BE} = base – emitter voltage, 0.6 to 0.7 V

R_4 = current - sensing resistance

Power supply characteristics

- Load regulation
- Source regulation
- Output Impedance
- Ripple Rejection

Fixed Regulator in market



Modulation

Introduction

Possible way to transmit speech and music

- Convert speech or music into electrical signal and transmit with a help of antenna.
- Receiver antenna can pick these signals and fed them to a loudspeaker to reproduce speech or music

- Problem
  - Energy of audio signal is low and can not be efficiently radiated. It will die out after covering even a small distance
  - If different transmitting station make transmission simultaneously, receiver antenna will pick all the singnal and it will lead to confusion

Contd.

- Solution
  - Audio signal superimposed on the high frequency carrier wave and then transmit. This process is called ***modulation***.

    The audio signal is called ***modulating wave*** and the signal obtained on superimposing it on carrier waves is called ***modulated wave,*** which is of high frequency

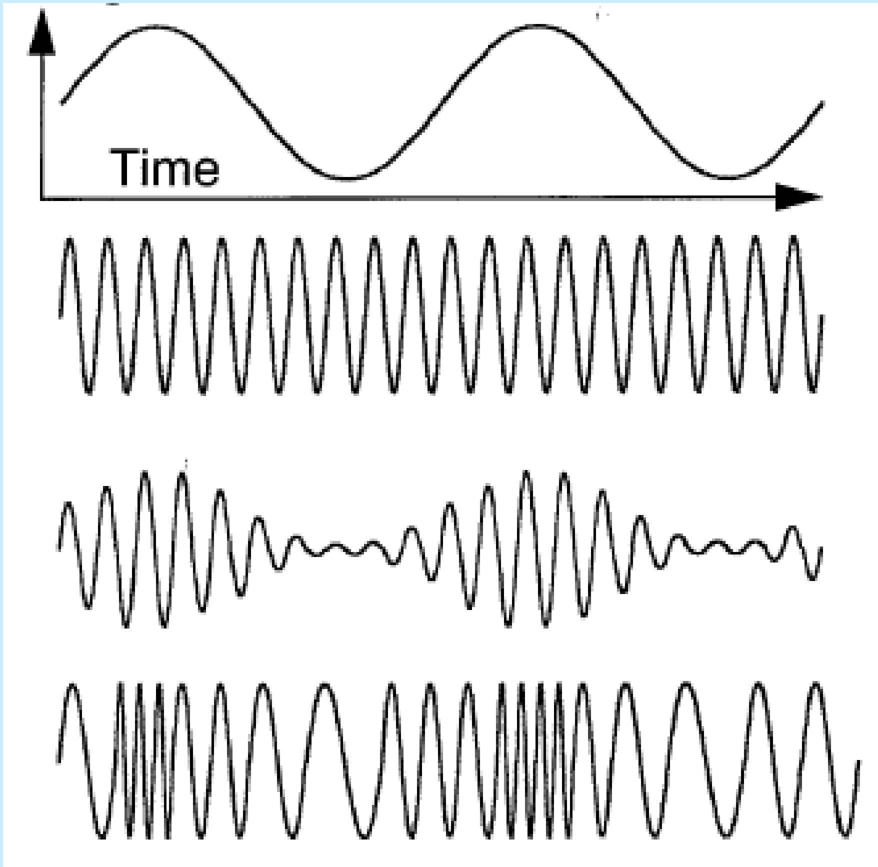
Modulation types

Signal

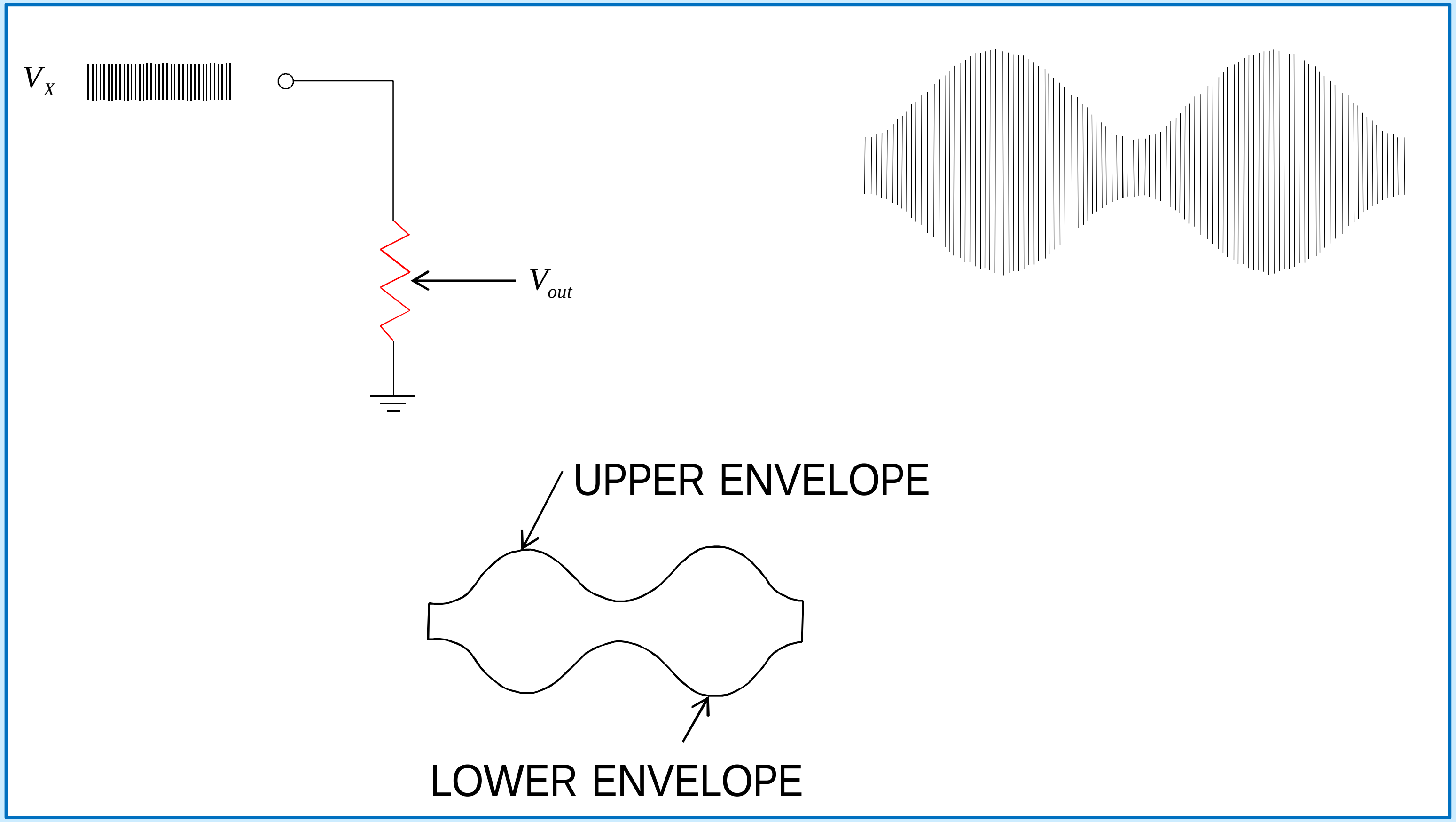
Carrier

Amplitude modulated

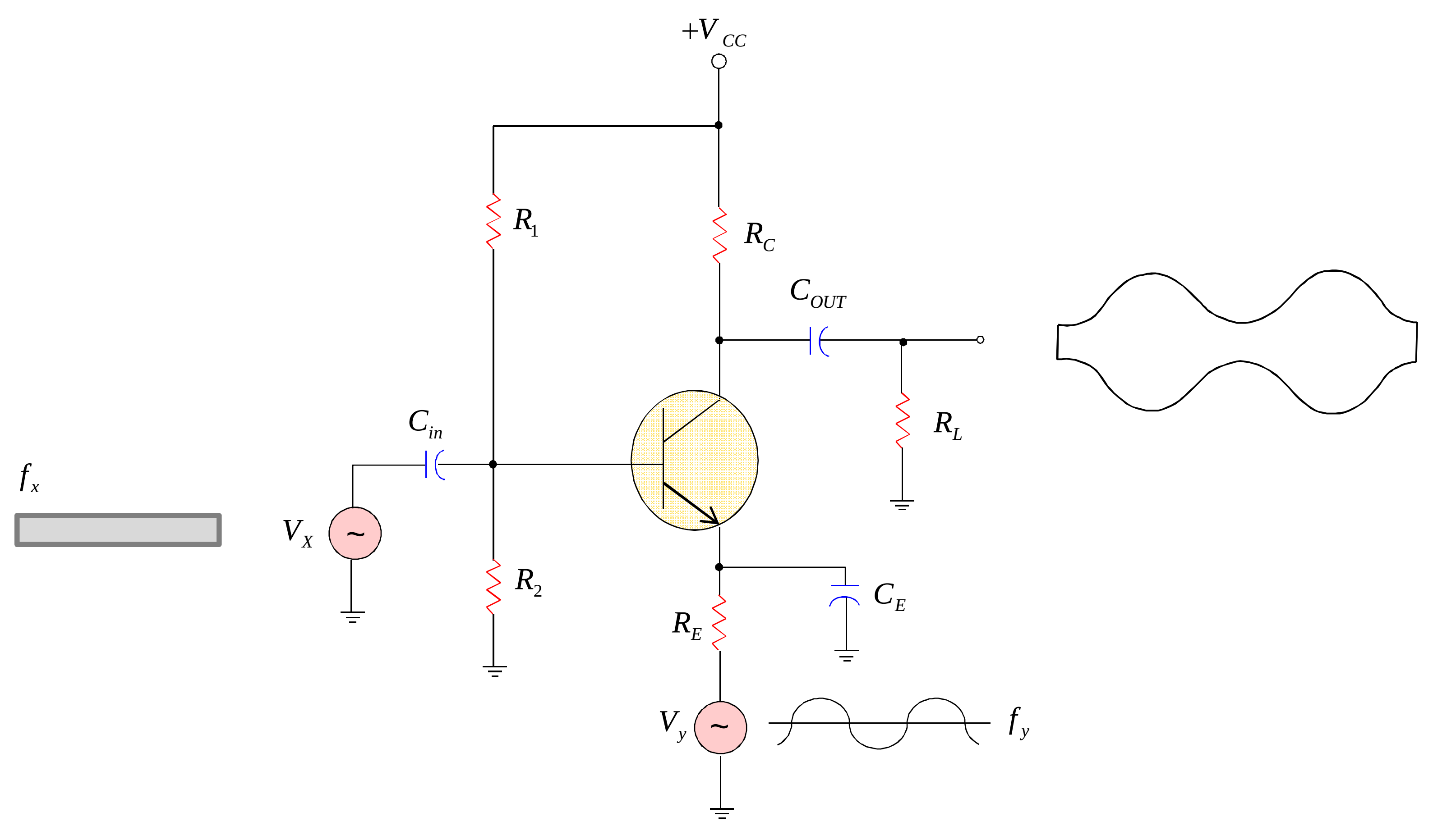
Frequency modulated



Simple Amplitude Modulation



Example of amplitude modulated RF stage



Percent modulation

Sinusoidal modulating stage produce sinusoidal variation in voltage gain expressed by

$$A = A_0(1 + m \sin \omega_y t)$$

A = instantaneous voltage gain

A_0 = quiescent voltage gain

m = modulation coeffiecient

Voltage gain varies between $A_0(1-m)$ and $A_0(1+m)$

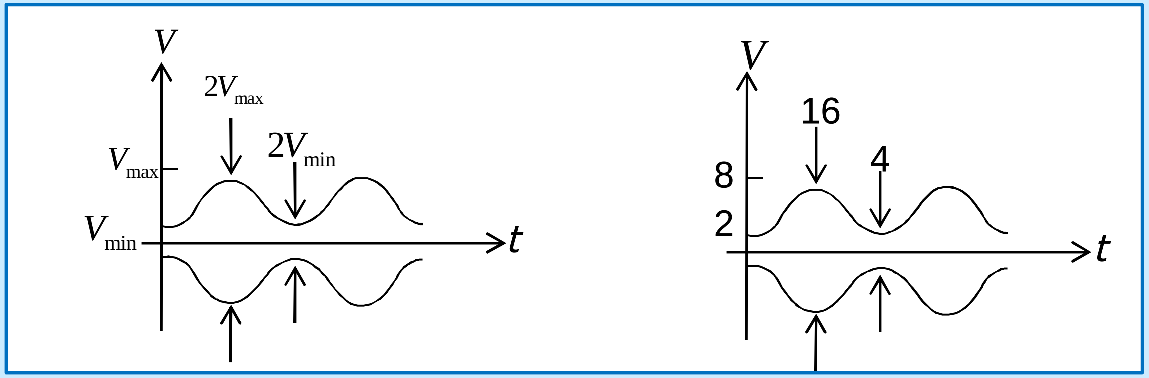
$$A_{\min} = 100(1-0.5) = 50$$

if $A_0 = 100$ and $m = 0.5$

$$A_{\max} = 100(1+0.5) = 150$$

Modulation percent

$$\text{Percent modulation} = m \times 100\%$$



$$m = \frac{2V_{max} - 2V_{min}}{2V_{max} + 2V_{min}}$$

$$m = \frac{16-4}{16+4} = 0.6$$

AM spectra

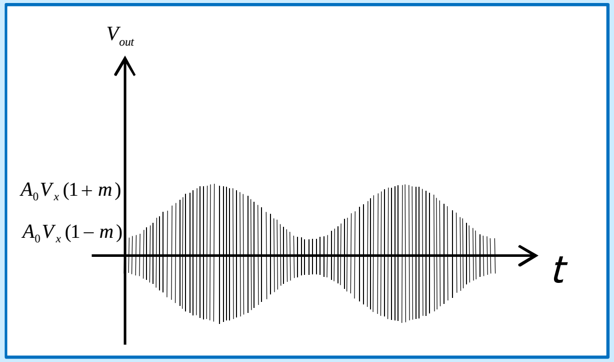
$$\upsilon_{out} = A\upsilon_x$$

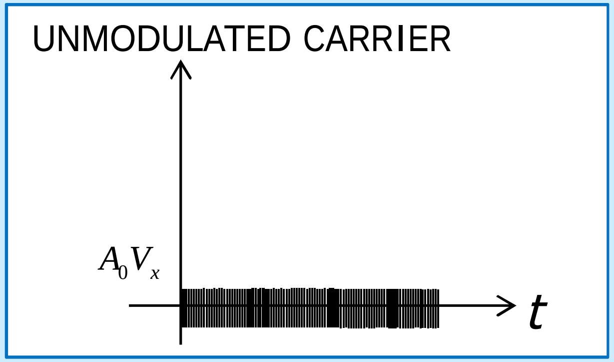
$$\upsilon_{out} = AV_x \sin \omega_x t$$

$$\upsilon_{out} = A_0(1 + m \sin \omega_y t)(V_x \sin \omega_x t)$$

$$\upsilon_{out} = A_0 V_x \sin \omega_x t + mA_0 V_x \sin \omega_y t \sin \omega_x t$$

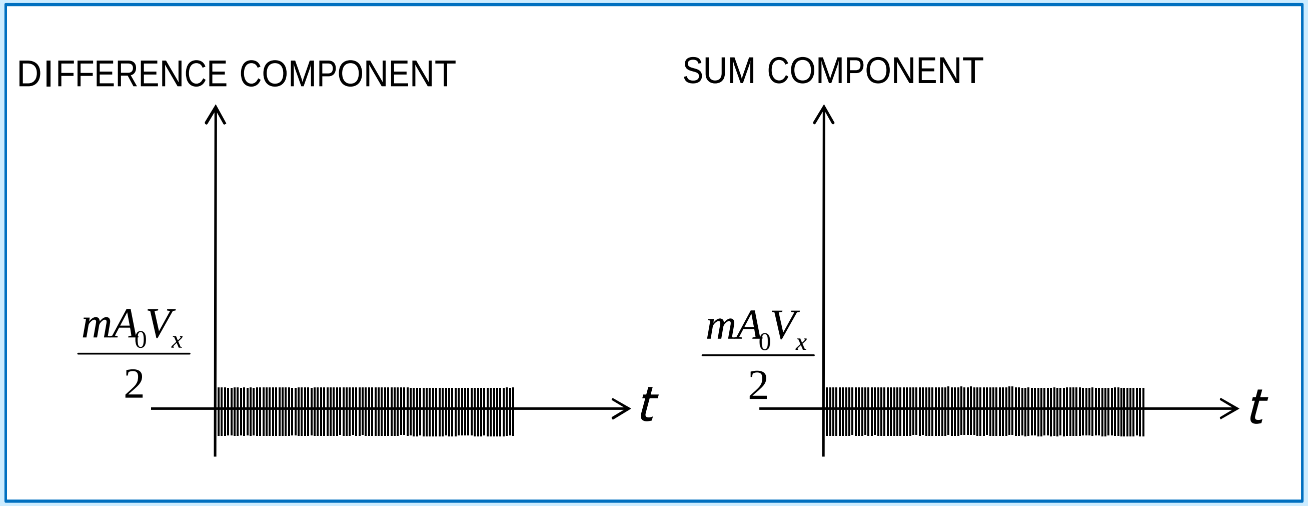
$$mA_0 V_x \sin \omega_y t \sin \omega_x t = \frac{mA_0 V_x}{2} \text{COS}(\omega_x - \omega_y)t - \frac{mA_0 V_x}{2} \text{COS}(\omega_x + \omega_y)t$$



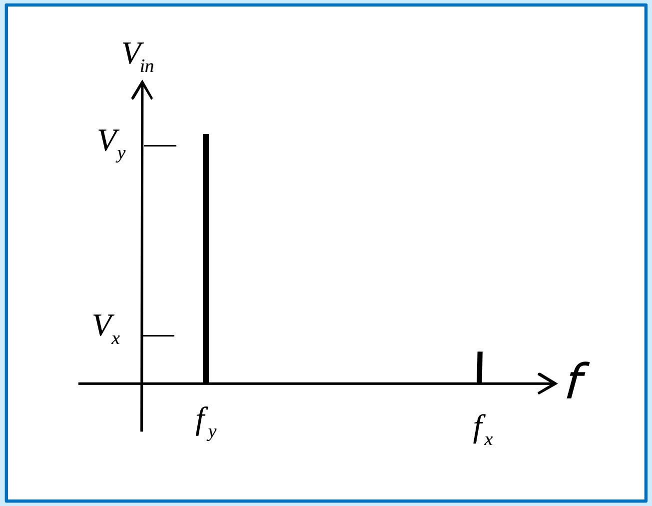


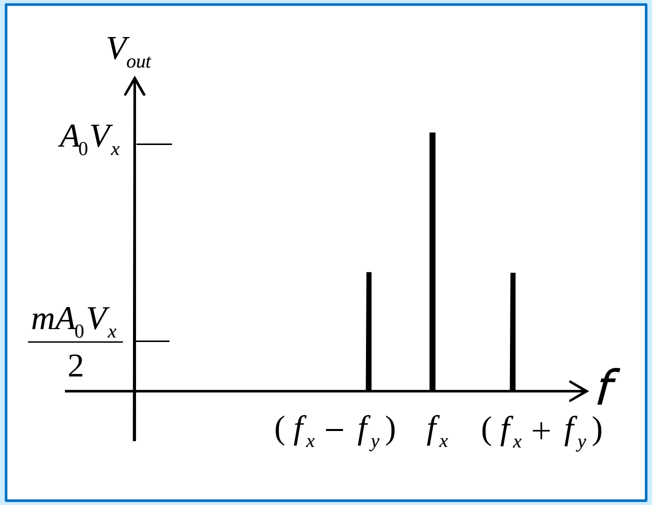
$$\upsilon_{out} = A_0 V_x \sin\omega_x t + mA_0 V_x \sin\omega_y t \sin\omega_x t$$

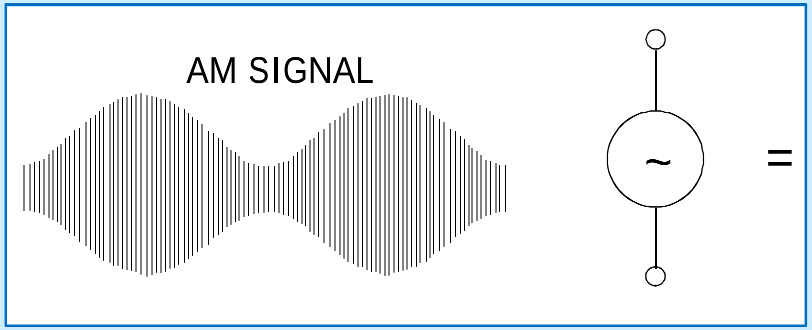
$$mA_0 V_x \sin\omega_y t \sin\omega_x t = \frac{mA_0 V_x}{2} \cos(\omega_x - \omega_y)t - \frac{mA_0 V_x}{2} \cos(\omega_x + \omega_y)t$$

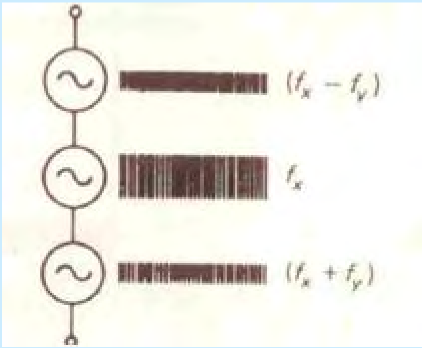


Spectral components



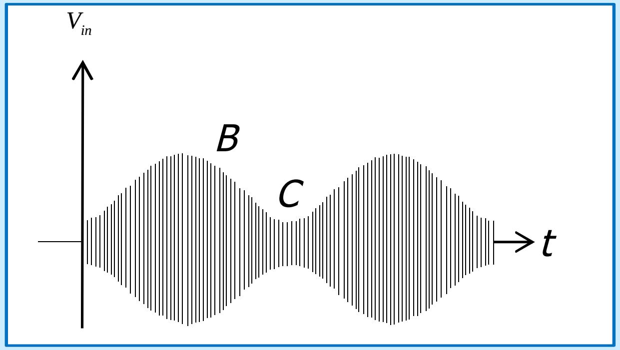


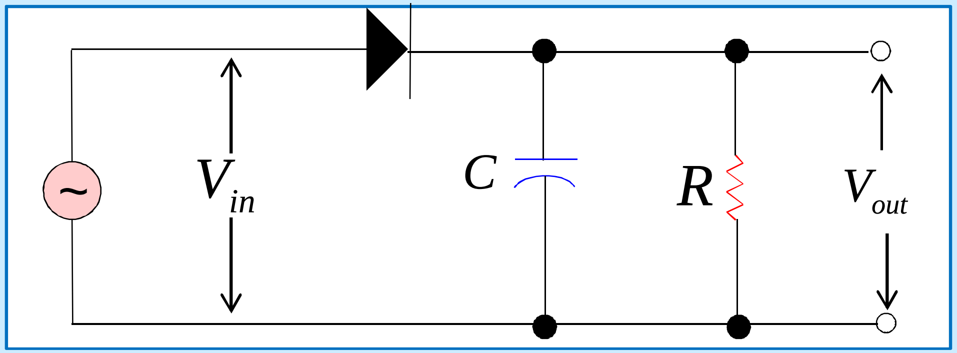


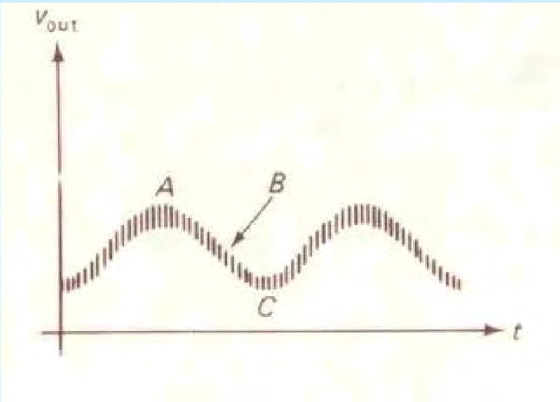


Demodulation

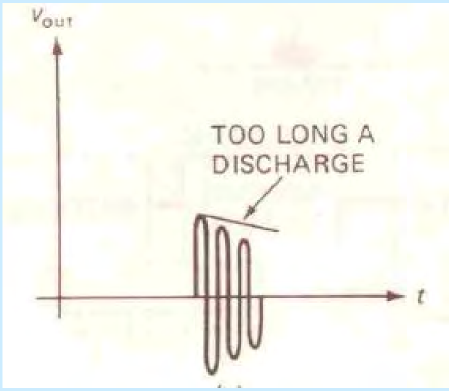
- Envelop detector
  - Peak detector by diode







RC time constant function of m



THE END

Wish you all the best